More Compute Changes

1. What are the New Big Events of 1994?

Low-cost versions of shared memory computers are in style. The chips are delivering 0.2 to 0.35 of a Y-MP processor, and machines with 8 or 16 processors are being purchased. About April 1995 a Cray Jedi will be available, and each processor will deliver 0.6 of a Y-MP processor. The cost of computing is coming down rapidly. For these options, the task of programming is about the same as for big computers; the difficulty of present parallel designs is avoided.

And the big news is that NCAR is in the process of obtaining much more computer power. The lack of power has been limiting the ability to develop and run climate models, mesoscale models, and other models.


This summarizes the main power at NCAR that has been available to NCAR or university users of main computers. Figure 1 shows how the amount of computing power at NCAR has been changing from 1975-on.

<table>
<thead>
<tr>
<th>Computer power May 1971-77</th>
</tr>
</thead>
<tbody>
<tr>
<td>The CDC 7600 and CDC 6600 (the CDC 7600 is 5 times the speed of the CDC 6600, a precise speed gain)</td>
</tr>
<tr>
<td>Power (in Y-MP processor equivalent)</td>
</tr>
<tr>
<td>0.1</td>
</tr>
</tbody>
</table>

2.2 Computer power 1977 to May 1983

One Cray 1A and CDC 7600. The Cray 1A was 4.5 times the speed of the CDC 7600 on average, about 2.4 times the speed in serial code. The average production gain was likely to be 3.5 times.

2.3 Computer power May 1983 to Sep 1986

Two Cray 1As (X-MP processor is 2 times the Cray 1) 0.71

2.4 Computer power Oct 1986 to May 1990

X-MP (4 processors), and Cray 1A (Y-MP processor is 1.4 times the X-MP1) 3.2
2.5 Computer power Jun 1990 to early 1994

Y-MP8 (8 processors) came May 1990;  
Y-MP2 (2 processors) came Jun 1991

2.6 Computer power May 1994

- Y-MP8 (came May 1990) and Y-MP2 (Jun 1991)  10.0
- Cray 3, 1 processor, used 55% (1.5 times  
  the speed of a Y-MP1)  0.8
- IBM cluster (1 - 550 and 2 - 590)  0.8
- Connection machine, CM-5 (32 node, used 50%)  0.6
- IBM SP1, 8 processors, used 50%  0.2
  TOTAL 12.4

Power  
(in Y-MP processor equivalent)

2.7 Computer power Oct 1994

- 2 Y-MPs, 8 processors each  16.0
- 3 Cray ELs, 8 processors each (0.21 Y-MP ea)  5.0
- Cray 3, 2 processors (each 1.5 Y-MP)  3.0
- IBM cluster (1 - 550 and 3 - 590s) (0.10, 0.33)  1.1
- Cray T3D (32 node, 64 processors)  2.1
  (use 0.22 per node and 0.3 efficiency)
- Connection machine, CM-5 (32 node, used 50%)  0.6
- IBM SP1, 8 processors (each 0.14, less in parallel)  0.3
  TOTAL 28.1

2.8 Power estimate for Apr 1995 (update Cray ELs to Jedi)

Power  
(in Y-MP processor equivalent)

- 2 Y-MPs, 8 processors each  16.0
- 2 Cray Jedi's, 16 processors each (0.60 Y-MP each)  19.2
- Cray 3, 2 processors each (1.5 Y-MP each processor)  3.0
- IBM cluster (1 - 550 and 3 - 590s)  1.1
- Cray T3D (32 node), better software  2.4
- Connection machine, CM-5 (32 node)  0.6
- IBM SP1, 8 processors  0.3
  TOTAL 42.6
2.9 Power estimate for Nov 1995

Either the T3D will be replaced by a Y-MP8 (8 processors),
or it will give more power (use 4.5 Y-MP processors)

TOTAL 44.7

2.10 Some notes about computer power not at NCAR now

Notes: (1) Many labs have a Cray C-90 computer with 16 processors. What is the
power of one of these? One C-90 processor has the power of 2.15 Y-MP
processors. Therefore, 16 C-90 processors are equal to 34.4 Y-MP
processors.

(2) A Cray 4 option: Suppose that Seymour Cray can build an 8-processor
Cray 4 and sell it for $4 million, as he claimed in Computerworld (Jul
18, 1994) (maybe it could be ready about Sep 1995?). How much power
would this 8-processor computer have? Each processor will probably be
about twice as fast as a C-90 processor. Therefore an 8-processor Cray 4
would be equivalent to about 32 or 33 Y-MP processors. (Same power
as the C-90 with 16 processors.) The total cost would probably be $6
million over a 4-year period, or $1.5 million per year. This 4-year cost
is the same as $47,000 per Y-MP processor each year. Will this really
happen; would the price be this low?

(3) A Cray Research Triton option: The Triton should be about the same
speed as the Cray 4. My guess is that the development is a little ahead
of the Cray 4. I do not have any price estimates.

2.11 Comments about cost

- The 3-year cost of the Cray ELs and the 2 Jedi's: The cost to NCAR (spread over
3 years and four payments) is $2.7M. The last payment of $700K is in Oct 1996,
and then NCAR will own the computers. This money buys NCAR an average of
15 Y-MP processors of power, with maintenance and software for 3 years, starting
July 1994. Over 3 years, the cost is about $60K each year per Y-MP of power.
Taken over 4 years, the cost would be even lower. (NCAR is obtaining this
equipment.)

- The new Y-MP8 and T3D: The 3-year cost (with maintenance) is $9.6M ($3.2M
per year starting July 1994). This is for an average of power of 11 Y-MP
processors (8 on the Y-MP and 3 on the T3D). At the end of 3 years, NCAR
would have to pay an additional $900K to own the computers. By Oct 1995, either
the T3D will deliver 8 Y-MP processors or NCAR has an option to have another
Y-MP8 instead of the T3D. The 4-year cost (with maintenance) would be about
$10.8M for an average of 12 Y-MP processors (or $225K per Y-MP processor
each year). (NCAR has obtained this equipment.)
Figure 1. Computer power at NCAR from 1975-95 (in Y-MP processors). This is the amount of high-end real output computer power (not peak power). It does not include many smaller workstations. The power is measured in the equivalent power of Cray Y-MP processors.
• The combined cost of the above two contracts is $4.1M per year.

• The silicon graphics option (Oct 1994). Obtain a 16-processor shared memory computer with the R8000 chip for a cost of about $831K plus 22K per year for maintenance. Over 3 years, the cost would be $300K per year for a power of 5.6 Y-MP processors. This is the same as a cost of $53.6K per Y-MP processor each year. Note that this cost is only a little lower than the Cray Jedi option. SGI has been making some very interesting computers.

• The IBM SP2 option had 32 processors (each about 0.34 power of the Y-MP1). It is a parallel computer. The option of the IBM SP2 (for Jul 1994 that NCAR didn't get) would have delivered an average of 11.0 Y-MP processors of power for $800K per year for 3 years ($75K each Y-MP processor, each year). In parallel mode, it would have given only about 2.7 Y-MP processors of power. This assumes that in parallel mode we could achieve 25% of the output using single processor mode (parallel mode was the intended use). The cost of this computing (parallel mode) is about $300K per equivalent Y-MP processor each year.

• Option for the Cray C-90. NCAR has not had the amount of money that it would take to buy a C-90. Also, the cost per unit of computer power now (Oct 1994) seems rather high. NMC obtained a C-90 in Dec 1993. Their 5-year lease cost with maintenance and finance charges was $46M (about $9M per year). This 5-year cost is equal to $267K per Y-MP processor each year. This is very high compared with other options. However, it probably includes some costs that are not included in other options.

• Cost of NCAR Y-MP8 obtained May 1990: The cost with maintenance, spread over 8 years, is $3.2M a year (not including prior debt). This is $400K per Y-MP processor, per year...for many years. If the cost were spread over 4 or 5 years, the annual cost would be higher.

• Comparison with the Cray 1A of long ago. NCAR purchased a Cray 1A in 1976 for a cost of $8.86M; maintenance was about $450K per year. The cost with maintenance comes to about $2.7M per year, taken over 4 years (NCAR really had it a lot longer). This is a cost of $7.7M each year for one Y-MP processor equivalent of power. Also these are 1977 dollars that are each worth 2.2 times as much as a 1994 dollar.

• Prices change with time. When thinking about these costs for computing, we should remember that the cost of a given amount of computing power has been decreasing rapidly for many years (a decrease of about 30% each year). A rule of thumb is that after about 18 months, a user can buy twice the computing power for the same cost as earlier.
3. **Cray Computer Comparisons**

A comparison of the Cray computers at NCAR in Sep 1994 is shown in Figure 2. The Y-MPs are the bigger Crays at NCAR, and have a cycle time of 6 ns. The smaller Cray ELs have a cycle time of 30 ns. Timing tests on the ELs show that an EL processor has about 0.21 of the power of a Y-MP processor. This is close to what one would expect from the difference in cycle times alone (0.20). The Jedi upgrade to the ELs (about April 1995) will have a cycle time of 10 ns. It appears very likely that an EL Jedi processor will have the power of 0.6 of one Y-MP processor. This is impressive!

We will compare the power of single processors for selected Cray computers:

<table>
<thead>
<tr>
<th>Year</th>
<th>Computer</th>
<th>Cycle time</th>
<th>Comment</th>
<th>Power (Y-MP Equivalent)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1971</td>
<td>CDC 7600</td>
<td>27.0 ns</td>
<td>5.0 times a 6600</td>
<td>0.10</td>
</tr>
<tr>
<td>1977</td>
<td>Cray 1A</td>
<td>12.5 ns</td>
<td>3.5 times a 7600</td>
<td>0.35</td>
</tr>
<tr>
<td>Oct 1986</td>
<td>Cray X-MP</td>
<td>8.5 ns</td>
<td>2.0 times a Cray 1A</td>
<td>0.71</td>
</tr>
<tr>
<td>May 1990</td>
<td>Cray Y-MP</td>
<td>6.0 ns</td>
<td>1.4 times a X-MP</td>
<td>1.0</td>
</tr>
<tr>
<td>--</td>
<td>Cray C-90</td>
<td>6.0 ns</td>
<td>2.1 times a Y-MP</td>
<td>2.1</td>
</tr>
<tr>
<td>Oct 1994</td>
<td>Cray EL98</td>
<td>30.0 ns</td>
<td></td>
<td>0.21</td>
</tr>
<tr>
<td>Apr 1995</td>
<td>Cray Jedi*</td>
<td>10.0 ns</td>
<td></td>
<td>0.60</td>
</tr>
</tbody>
</table>

* This power is an estimate made in Oct 1994.

**Notes:**

1. Overall, the Cray 1A was 4.5 times a CDC 7600. However, main models on the 7600 had special coding so that it almost acted like a vector computer. The real production increase for NCAR was probably a factor of 3.5.

2. In Oct 1986, NCAR got the first X-MP with a cycle time of 8.5 ns. The cycle time on earlier X-MPs was 9.5 ns.

4. **Some Memory Comparisons**

The amount of memory on selected main computers at NCAR has been:

<table>
<thead>
<tr>
<th>Computer</th>
<th>Words</th>
<th>Bits/Words</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDC 7600 (1971)</td>
<td>64 Kword</td>
<td>60</td>
<td>512 Kword large memory</td>
</tr>
<tr>
<td>Cray 1A (1977)</td>
<td>1 Mword</td>
<td>64</td>
<td>No SSD</td>
</tr>
<tr>
<td>Cray X-MP (1986)</td>
<td>8 Mword</td>
<td>64</td>
<td>SSD with 256 Mword</td>
</tr>
<tr>
<td>Cray Y-MP (1990)</td>
<td>64 Mword</td>
<td>64</td>
<td>SSD with 256 Mword</td>
</tr>
<tr>
<td>Cray EL98 (1994)</td>
<td>256 Mword</td>
<td>64</td>
<td>No SSD</td>
</tr>
<tr>
<td>Cray Jedi (1995)</td>
<td>256 Mword</td>
<td>64</td>
<td>No SSD</td>
</tr>
</tbody>
</table>

The cost of memory has decreased drastically so that large amounts of it are now much more affordable.
## Cray Computer Comparisons

<table>
<thead>
<tr>
<th>Computer Type:</th>
<th>(Y-MP8)</th>
<th>(EL98)</th>
<th>(EL98)</th>
<th>(EL92)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Computers:</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>NCAR Computer Names:</td>
<td>Shavano &amp; Antero</td>
<td>Alpine &amp; St. Elmo</td>
<td>Monarch</td>
<td>Echo</td>
</tr>
<tr>
<td>No. of CPUs:</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>2</td>
</tr>
<tr>
<td>Clock:</td>
<td>6 ns</td>
<td>30 ns</td>
<td>30 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>Memory:</td>
<td>64 MW (512 MB)</td>
<td>256 MW (2048 MB)</td>
<td>128 MW (1024 MB)</td>
<td>64 MW (512 MB)</td>
</tr>
<tr>
<td>SSD:</td>
<td>256 MW</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Disk:</td>
<td>99 Gbyte</td>
<td>46 Gbyte</td>
<td>46 Gbyte</td>
<td>21 Gbyte</td>
</tr>
</tbody>
</table>

Notes: (1) The above Cray computers are at NCAR in Sep 1994.
(2) The two Jedi's will have a clock cycle of 10 ns. They will arrive about April 1995 and replace three EL computers. The two Jedi computers will each have 16 processors and 2048 MB of memory.

Figure 2. Cray computer systems at NCAR in Sep 1994. There are six Crays and this shows the configuration of each of them. Each Y-MP has 8 processors and a 256-Mword SSD (solid state disk). Each EL processor is 0.21 the speed of a Y-MP processor (similar to the cycle time difference). Gene Schumacher gathered most of these numbers.
The system costs for the computers were:

1) CDC 7600, $8.2M
2) Cray 1A in 1976, $8.86M
3) Cray X-MP (4 processors, 1986), $20.1M with SSD

5. Computer Output versus Speed of One Program

At NCAR we should normally try to optimize the output of important model results from the computers, and worry somewhat less about how fast one model can run. The efficiency of the use of processors usually drops as more processors are used on one job. This is one of the factors that should be included when deciding on how many processors to use on one job. For example, the timing of the NCAR CCM2 climate model on the SGI computer with R8000 chips (a shared memory computer) is as follows:

<table>
<thead>
<tr>
<th>Number of Processors</th>
<th>R8000 time</th>
<th>Speedup</th>
<th>Processor Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>999 sec</td>
<td>1.00 x</td>
<td>100%</td>
</tr>
<tr>
<td>4</td>
<td>281</td>
<td>3.56 x</td>
<td>89%</td>
</tr>
<tr>
<td>8</td>
<td>164</td>
<td>6.09 x</td>
<td>76%</td>
</tr>
<tr>
<td>12</td>
<td>334</td>
<td>7.46 x</td>
<td>62%</td>
</tr>
<tr>
<td>16</td>
<td>111</td>
<td>9.0 x</td>
<td>56%</td>
</tr>
</tbody>
</table>

From this chart we see that if we use all 16 processors on this job, we only use the processors at an efficiency of 56%. In other words, we give up 44% of the potential output of the computer. To try to maximize the output, it will often make better sense to use only 4 or 8 processors on one job and run several jobs in parallel.

NCAR is almost always running 5 to 20 big model jobs at the same time. It is a bad bargain to try to run one job a little faster, if at the same time we obtain markedly less total output from the computer.

6. The New Sun UltraSPARC Chip

Sun Microsystems has fallen behind in the pace for RISC chip performance for several years. The Sun Super-SPARC is not only slower than the RISC chips, but also slower than the Intel Pentium (at least in integer performance). The Pentium is being used in millions of PCs.

The UltraSPARC chip will help, with SPECint 92 benchmarks ranging from 200 to 400 (article in Computerworld by Jean Bozman, Sep 26, 1994).

7. The IBM 590 Computer

The University of Arizona has been running the full NCAR climate model, CCM2, with the surface code called BATS on an IBM 590 computer in 64-bit precision. The resolution is
T42 (2.81° grid) with a 20-min time step. This computer takes 3.5 times more CPU time than one processor of a Y-MP (it therefore is 0.29 of a Y-MP).

8. The Cray T3D Computer

The Cray T3D is a parallel computer. The T3D uses a 150-MHz (6.67 ns) Dec Alpha chip (called the 21064-AA (EV-4)). There are two of these processors in each of the 32 nodes at NCAR. The next upgrade, the T3E, will have the EV-5 chip (only one per node). Cray plans a new MPP about each 2 years. The letters MPP mean massively parallel processor.


Paul Swarztrauber's advanced computing section at NCAR has made enough tests on the Cray T3D to have an estimate of how fast it will be able to run the climate model CCM2. It should be able to deliver 8 to 10 Mflops per processor (or 16 to 20 per node). The total output from 64 processors would therefore be 500 to 650 Mflops. This is nearly the same as 4 Y-MP processors (CCM2 runs at 150 Mflops on one Y-MP processor). However, when the T3D runs, one Y-MP processor is tied up.

The NCAR contract with Cray says the combination of the Y-MP8 and the T3D must equal the output of 12 Y-MP processors. If it is less than this, Cray can either improve the T3D so that the total power of 12 Y-MP processors is delivered, or a second Y-MP8 would be installed, done by about Oct 1995. It is best to bet on 12.5 processors of power. With two Y-MP8s, we would have 16 processors.

10. GFDL Plans to Obtain Another Computer (written Oct 1994)

GFDL obtained a Cray Y-MP8 computer in 1990, the same year that NCAR got one. They recently made their last annual payment of $5.5 million on the Y-MP and are in the market for a faster computer and associated storage gear. The GFDL computers are mostly used for climate modeling. Since the U.S. badly needs better climate estimates there is a move to supply the additional computer power that is necessary. GFDL's total budget is around $14 million per year, and half of that ($7 million) goes for computing. Computing is very important to the work needed, so they have to spend this high fraction of the budget on it. The GFDL director, G. Mahlman, points out that in most ways GFDL is very similar to the climate division (CGD) at NCAR. GFDL will obtain the new computer about summer 1995. The bidding process is very open.

The situation with the first NCAR Y-MP8 (got in 1990) is worse. The last payment (of $3.8 million) is still a long ways off — Dec 1996.

11. Some Fast Chip Comparisons

It is useful to describe how fast some of the single CPU chips will run major model codes in comparison to one Cray Y-MP processor. The CCM2 is the main climate model at NCAR. Some comparisons are:
<table>
<thead>
<tr>
<th>Date of Products Having Chip</th>
<th>Type of CPU</th>
<th>Timing vs. Y-MP1</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990 at NCAR</td>
<td>Cray Y-MP processor</td>
<td>1.0</td>
<td>on CCM2 model</td>
</tr>
<tr>
<td>Aug 1994</td>
<td>Cray EL 98</td>
<td>0.21</td>
<td>on CCM2</td>
</tr>
<tr>
<td>Mar 1995</td>
<td>Cray Jedi</td>
<td>0.6</td>
<td>on CCM2</td>
</tr>
<tr>
<td>Dec 1993</td>
<td>IBM 590</td>
<td>0.29</td>
<td>on CCM2 (use 0.34 in general)</td>
</tr>
<tr>
<td>Aug 1994</td>
<td>SGI R8000</td>
<td>0.29</td>
<td>on CCM2 (use 0.35 in general)</td>
</tr>
<tr>
<td>est. May 1995</td>
<td>Alpha 21164 (300 MHz)</td>
<td>0.48 (est.)</td>
<td>on CCM2</td>
</tr>
<tr>
<td>~ 1992</td>
<td>Cray C-90</td>
<td>2.15</td>
<td>not at NCAR</td>
</tr>
<tr>
<td>~ late 1995</td>
<td>Triton or Cray 4</td>
<td>4.2 (est.)</td>
<td>estimates</td>
</tr>
<tr>
<td>mid 1996</td>
<td>Some fast chips</td>
<td>0.9 (est.)</td>
<td></td>
</tr>
</tbody>
</table>

*Note:* This table was prepared October 1994

12. **The Cost of Disk Space**

The disk investment cost per megabyte and the speed are summarized below:

<table>
<thead>
<tr>
<th>Disk</th>
<th>Mbyte</th>
<th>Cost</th>
<th>Cost/Mbyte</th>
<th>Data Speed Access/Rate (Mbyte/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1977 DD19</td>
<td>303</td>
<td>$60,000</td>
<td>$198</td>
<td>50 ms/4.43</td>
</tr>
<tr>
<td>1986 DD49</td>
<td>1219</td>
<td>140,000</td>
<td>115</td>
<td>16/10.3</td>
</tr>
<tr>
<td>1984 IBM 3380</td>
<td>5000</td>
<td>140,000</td>
<td>28</td>
<td>-/3.0</td>
</tr>
<tr>
<td>1990 (May) DD4R</td>
<td>5200</td>
<td>250,000</td>
<td>48.08</td>
<td>13/9.6</td>
</tr>
<tr>
<td>1988 PC disk</td>
<td>720</td>
<td>4,450</td>
<td>6.20</td>
<td>14/1.0</td>
</tr>
<tr>
<td>1991 (Dec) PC disk</td>
<td>1350</td>
<td>2,800</td>
<td>2.07</td>
<td>14/1 to 4.0</td>
</tr>
</tbody>
</table>

13. **Measured Changes in Electricity Power Use**

NCAR measured the following changes in steady power use as computing equipment was changed.

<table>
<thead>
<tr>
<th>Date</th>
<th>Change in Power Use</th>
<th>Old kW</th>
<th>New kW</th>
<th>Change kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>27 May 1994</td>
<td>Turn off the Cray 3 (4 processors; 1 was used)</td>
<td>702</td>
<td>581</td>
<td>-121 kW</td>
</tr>
<tr>
<td>3 Jun 1994</td>
<td>Turn off 2-processor Y-MP (Mecca)</td>
<td>580</td>
<td>505.6</td>
<td>-74.4 kW</td>
</tr>
<tr>
<td>5 Jun 1994</td>
<td>Turn on new Y-MP8, 64 (has 5 processors)</td>
<td>496</td>
<td>601</td>
<td>+105 kW</td>
</tr>
<tr>
<td>19 Jul 1994</td>
<td>Turn on T3D (32 nodes)</td>
<td>408</td>
<td>447</td>
<td>+39 kW</td>
</tr>
<tr>
<td>21 Sep 1994</td>
<td>Change 5-processor Y-MP8 to 8 processors</td>
<td>628</td>
<td>645</td>
<td>+17 kW</td>
</tr>
<tr>
<td>23 Sep 1994</td>
<td>Turn on Cray 3 (2 processors)</td>
<td>528</td>
<td>552.4</td>
<td>+24.2 kW</td>
</tr>
</tbody>
</table>
Notes: (1) A Cray EL98 with 8 processors uses about 4 kW. The power of this computer is the same as 1.7 Y-mp processors.

(2) Oct 1994: There are two power stations for major computing at NCAR. With present equipment running, two stations measure 432 kW and 690 kW, for a total of 1122 kW. In addition, much cooled water is received from other power sources.

14. A Lot More Computing and Data; How is the Mass Store Doing?

There are now (Oct 1994) five physical data channels coming out of the mass store (MSS), and there will soon be six. These are 100 Mbit/sec (12.5 Mbyte/sec) HIPPI channels, but the data rate from the storage hardware is slower than this. The data channel rates from 3490 drives to their controllers is 3 MB/sec, but the data is compressed at this point. The compression at NCAR gives a 30% gain. We often see data rates from the controllers to/from users of almost 4.5 MB/sec. The result of all of this is that there will be very good data flow between the mass store, the two Y-mps and the Cray EL computers.

NCAR has tapes in a silo, with automatic mounting, and thousands of tapes on the floor (manual mounting). The silo now has 5411 tape cartridges and 16 tape drives (four of these were added Aug 1994). The tapes are double density and long. Each actually has 900 MB of data. There are another 16 drives on the floor for manual mounting.

How much data flow is there at NCAR? The user data flow to and from the MSS is now about 8 Tbytes per month (260 Gbytes per day). There is an additional internal data flow of 8 Tbytes per month to migrate data to where it belongs.

15. Summary of Data Flow to/from the NCAR Mass Store

Approximate data moved on the NCAR mass store

<table>
<thead>
<tr>
<th>Year</th>
<th>Writes (in MB/hr)</th>
<th>Reads (in MB/hr)</th>
<th>Total (in MB/hr)</th>
<th>Total (in GB/day)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990</td>
<td>1150</td>
<td>2800</td>
<td>3950</td>
<td>95</td>
</tr>
<tr>
<td>1992</td>
<td>2000</td>
<td>5000</td>
<td>7000</td>
<td>168</td>
</tr>
<tr>
<td>1993</td>
<td>2000</td>
<td>5500</td>
<td>7500</td>
<td>180</td>
</tr>
<tr>
<td>Sep 1994</td>
<td></td>
<td></td>
<td></td>
<td>260</td>
</tr>
</tbody>
</table>

The NCAR MSS is keeping up with the computing power as of Oct 1994. However, the new power isn't all being used yet and a significant increase in power will occur about April 1995. Some of the new storage hardware will be necessary to keep up with the amount of new data from models and observations, and to handle the required data flow rates.
16. New MSS Hardware is Nearly Ready for Sale

IBM has new cartridge tape technology (same size cartridges as 3490) that will hold 10 Gbytes each cartridge, and compression will add 30% or more to that. These drives will probably be ready to sell in mid-1995. People usually will obtain four drives and one controller as a unit. An NCAR guess of the price is about $100K for four drives and another $100K for the controller ($200K for each set of four drives).

A small IBM library will be obtained by NCAR in Dec 1994 to test the new storage systems. It will have two cartridge modules and hold 700 cartridges. Two of the present 3490 tape drives are included in the price of $150,000. A new drive (an IBM NTP drive) will be added when it becomes available in 1995. This unit will first be used for lots of tests of hardware reliability.

17. The Health of Computing Companies

The computing industry has not been having an easy time in the past 5 or 6 years. Technology has permitted the cost of a unit amount of computing power to drop rapidly and competition has ensured that the prices actually do drop. Even though the appetite for increased computer power grows very rapidly, it is hard for computing companies to gain enough sales (in dollars) to maintain staffing at previous levels. Everyone knows that companies like IBM and DEC have had to reduce employment. Thinking Machines (developer of the CM-2 and CM-5 parallel computers) recently went into bankruptcy. Kendall Square has had enormous difficulty and recently reorganized under new management. Cray Computer Corp. (with Seymour Cray) is looking for an investment partner. Cray Research is feeling the competition and losing staff, but is still quite healthy. Some companies from the late 1980s, such as Ardent and Stellar are gone.

The recession of 1991 and Defense Department budget cuts have made it harder for the industry. However, all is not bleak. The improving economy is a plus and there is increased need for computing in many sections of the economy.
Compute Updates

1. Obtain "Smaller" Cray EL Computers with Shared Memory

Cray Research has had the line of Cray EL computers for several years that have several processors with a shared memory. They are completely compatible with the bigger Crays, which is a big advantage in a Cray environment such as NCAR. The speed of one Cray EL98 or EL92 processor is 0.21 of one Y-MP processor. This is consistent with the clock times (30 ns versus 6 ns on the Y-MP). See Table ____. In May 1994, NCAR signed a contract to obtain the following:

- In summer 1994 NCAR obtained three Cray EL computers, each with 8 processors and 1024 MB of memory (128 Mwords). The combined power of all three computer is about 5.1 Y-MP processors (each EL processor is 0.21 of a Y-MP processor).
  - Two EL98s were obtained June 27, 1994. Each has 8 processors and 1024 MB of memory (128 Mwords). Each EL has 46 Gbyte of disks. In Nov 1994, one of these will have 256 MWords of memory.
  - One EL98 with 512 MB (64 Mwords) of memory and 21 GB of disks will come Aug 1, 1994.

- An upgrade of the ELs. About March 1995, the ELs will depart and NCAR will obtain two J916 computers each with 16 processors and 2048 MB of memory (256 Mwords). These are called Jedi computers. The clock speed is three times faster than the EL computers (10 ns versus 30 ns). The actual speed of one processor should be 0.6 of a Y-MP processor. Therefore the two Jedi's, each with 16 processors, will have a combined speed equal to 19.2 Y-MP processors. This power is more than the 16 processors on the two Y-MP8s at NCAR. The Cray ELs are also shared memory computers that are easy to use...like the Y-MP8s. These two computers will replace the three computers above.

- The 3-year cost for these three computers is about $2.7M (about $900K per year). The $2.7M contract includes maintenance cost of $143K per year. NCAR was able to obtain a large discount off of the list price. The 3 years started July 1994. The last payment of $700K is in Oct 1996. Then NCAR will own these computers.

2. How do Cray ELs talk to the Mass Store?

There is a separate HIPPI connection from each of the four ELs to the mass store. A HIPPI channel is rated at 100 mbit/sec (12.5 MB/sec). This is faster than the IBM storage gear can deliver data (Oct 1994). Tests on the bandwidth have been made. There will be no trouble in moving data between the ELs and the mass store.

3. MIPS Chips; the Silicon Graphics Option of August 1994

This computer is a shared memory computer like a Cray Y-MP with several processors. The chip speed was 100/50 MHz in summer 1993; by Nov 1993 users could obtain the 150/75
MHz chip. The next big jump in chip speed should be available about Aug 1994. A processor will have the power of about 0.29 to 0.35 Y-MP processors. If a user had a 4-processor computer, the power would be 1.3 Y-MP processors. One job could use all four processors and run at about 75% efficiency, giving a speed of about 1.2 Y-MP processors. These computers are available with 16 processors.


A 16-processor computer, based on the R8000 chip, can be obtained by NCAR at an attractive price (NCAR discount of about 35%). A sample configuration follows:

<table>
<thead>
<tr>
<th>Component</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 CPU Challenge XL</td>
<td>$526K</td>
</tr>
<tr>
<td>2 GB 8-way interleaved memory</td>
<td>138K</td>
</tr>
<tr>
<td>64 GB disk array</td>
<td>127K</td>
</tr>
<tr>
<td>I/O (HIPPI, FDDI, channels)</td>
<td>40K</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>$831K</strong></td>
</tr>
</tbody>
</table>

Annual software and hardware maintenance is only $22K, under a special agreement between NCAR and SGI.

The power of each processor is equivalent to about 0.35 Y-MP processors. The total power is therefore the same as 16 x 0.35, or 5.6 Y-MP processors. The information on costs was obtained from SGI by Don Middleton.

5. The Next MIPS Chip, the T5

The T5 is based on the same fifth generation super scalar RISC technology as in the R8000 that got into products about Aug 1994. The R8000 was mainly for high-end scientific calculations. The T5 has a more all-around flavor and will be used in workstations, PCs and servers. At its initial core speed of 200 MHz, it is expected to deliver 250 SPECint 92 and 350 SPECfp 92. This compares with 108 and 310 speeds for the MIPS R8000. The T5 has over 6 million transistors. It is based on 0.35 micron technology, using 3.3 volts. Most instructions use one cycle; a 32- or 64-bit floating point multiply, add, etc., uses two cycles. It has several instruction units including two FPUs. It will be in volume production by late 1995. The price is estimated at $1000 to $1200. For more information, see the four-page article in the Nov 1994 issue of BYTE magazine by Tom Halfhill.


Timing tests have been performed using the new MIPS 75 MHz R8000 processors, also known as TFP. One R8000 processor ran the community climate model (CCM2) at a speed of 45 Mflops, which is 0.29 of a Y-MP processor. This problem has been optimized for a Y-MP; on the average big problem, a R8000 processor is probably about 0.35 of a Y-MP processor.

The R8000 is 3.1 times faster than the previous fast MIPS processor, the 150 MHz MIPS R4400 (NCAR got computers with this 150-MHz chip about Dec 1993).
Jack Perry of SGI also completed timing tests on an ocean modeling code. The R8000 was 1/7th of a Cray C-90 processor. For the CCM2 model, a C-90 is 2.13 times the speed of a Y-MP processor.

On the NCAR climate model (CCM2), the SGI exceeded the power of one Cray Y-MP processor by using four R8000 processors, and it exceeded the speed of a Cray C-90 by using 12 processors. For these tests 16 processors were available in one shared-memory computer.

Some timing information about MIPS chips in SGI computers

<table>
<thead>
<tr>
<th>Available</th>
<th>Chip</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jul 1993</td>
<td>R4400/100 MHz</td>
<td>62 SPEC fp</td>
</tr>
<tr>
<td>Dec 1993</td>
<td>R4400/150 MHz</td>
<td></td>
</tr>
<tr>
<td>Aug 1994</td>
<td>R8000</td>
<td>310 SPEC fp</td>
</tr>
</tbody>
</table>

Information about the R8000 chip

- The R8000 chip is 3.1 times the speed of the R4400/150 MHz. It is 0.29 of a Y-MP1 on climate and ocean models.

7. SGI Power Challenge Performance on NCAR CCM2 Climate Modeling Code (June 20, 1994)

This is a report on the performance of the SGI Power Challenge system with the new MIPS 75 MHz R8000 processors, also known as TFP, in running the NCAR Community Climate Model, Version 2, (CCM2) provided to SGI by Florida State University along with a benchmark dataset. These are preliminary results achieved with pre-release versions of compilers, libraries, and operating system software. The SGI is a shared memory computer.

We began with a version of the code that had been previously ported and parallelized on the SGI Challenge system with 150 MHz R4400 processors. The parallelization changes consisted of converting the Cray microtasking directives to the equivalent forms of the SGI DOACROSS directive.

No changes in the code were made for the purpose of improving the performance of the R8000 processor, so the R8000 performance was exclusively due to processor speed as delivered through automatic compiler optimizations.

The table below shows the elapsed or wall time to run the job on various numbers of processors on a Challenge and Power Challenge system. The Challenge results are as previously reported by Charlie Taylor.
<table>
<thead>
<tr>
<th>Number of Processes</th>
<th>Challenge R4400 time (150 MHz)</th>
<th>Power Challenge R8000 time (75 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3112 sec.</td>
<td>999 sec.</td>
</tr>
<tr>
<td>4</td>
<td>895 sec. (3.48x)</td>
<td>281 sec. (3.56x)</td>
</tr>
<tr>
<td>8</td>
<td>475 sec. (6.6x)</td>
<td>164 sec. (6.09x)</td>
</tr>
<tr>
<td>12</td>
<td>391 sec.</td>
<td>134 sec.</td>
</tr>
<tr>
<td>16</td>
<td>287 sec. (10.8x)</td>
<td>111 sec. (9.0x)</td>
</tr>
</tbody>
</table>

*Note:* (9.0x) means speedup of 9.0 times versus 1-processor speed.

For comparison, the Cray speeds for the problem were supplied by FSU:

- Cray Y-MP (1 processor) = 155 Mflops, 290 seconds
- Cray C-90 (1 processor) = 330 Mflops, 136 seconds

On this major problem, note that:

- The R8000 is 3.1 times faster than the R4400 (150 MHz)
- The R8000 (1 processor) ran the job at a speed of about 45 Mflops.
- The R8000 (1 processor) speed is 0.29 of a Y-MP1, but this problem has been optimized for a Y-MP. On average, similar big jobs it is probably 0.35 of a Y-MP1 (comment by Jenne).
- The SGI Power Challenge exceeded the Cray Y-MP performance by using 4 processors, and the Cray C-90 performance (of 1 processor) by using 12 processors.
- One Cray C-90 processor is 2.13 times the speed of a Y-MP processor on this problem.
- For comparison, NCAR obtained a Cray X-MP (4 processors) in Oct 1986. The average Mflop rate was measured; it was 55 Mflops per processor, or 220 Mflops on the whole computer. The average rate applies to CPU time, not wall clock time (comment by Jenne).

The single processor times show the R8000 to be 3.1 times faster than the R4400 (150 MHz) on this benchmark. The parallel efficiency of the Power Challenge was slightly less than Challenge, because while the individual processor speed has significantly increased, the speed of synchronization and data movement across the memory bus has not increased.

The CCM2 code uses about 80 MB of memory for program text and data. The high parallel efficiency demonstrates that the 4 MB cache of the R8000 is very effective in reducing processors' need for main memory bandwidth, even when the dataset is considerably larger than cache size. All of the CCM2 calculations were done with 64-bit precision on the R8000.
Note: This message has been edited some. It was from David Baumgartner (dnb@pumphouse). This message was received via John Scanlan of Silicon Graphics, Denver.

Comment by John Scanlan, SGI: This result is noteworthy in that it is a large application code (~60K lines) which has been coarse-grain parallelized, and as a result we can beat the Cray C90 single processor time! I added the last paragraph to counter the supercomputists who claim that RISC cache machines can't perform on large supercomputer problems and that our memory bus is an obvious bottleneck.

Credit goes to Charlie Taylor and David Chen for their earlier work parallelizing this for Challenge.

8. Timing of an ocean model on the SGI R8000 chip

Jack Perry, SGI, says the following (June 1994):

I also ported a Cray Ocean Modeling code this week which had about a 70 MB dataset and a single R8000 was around 1/7 of C90 performance, similar to the CCM2 result (64-bit arithmetic on both SGI and Cray). I know there are a lot of skeptics in the supercomputing community about how well RISC cache architectures do on real applications with datasets much larger than even a 4 MB cache. It's been my expectation all along that vectored codes will perform well on this machine without restructuring into blocked algorithms because there is a moderate amount of data reuse in vector loops.

My experience in the past month of benchmarking has been that this machine (R8000) is not memory bandwidth limited on any of the 14 codes I have worked on, which include CFD, Molecular Dynamics, FEA, Crystallography, and climate, weather, ocean and river sediment modeling. It is almost always limited by the speed of reads and writes between the processor and the cache which is 1.2 GB/sec per processor.

Thanks for the interest,
Jack

Jack (John R.) Perry   jperry@sgi.com
Eastern Technology Center
Silicon Graphics, Inc.
One Cabot Road
Hudson, MA  01749
508-562-4800

9. What do Scientists Think about Parallel Computing?

Bill Buzbee summarized attitudes of PIs toward parallel computing on 19 April 1994. Scientists are not enthusiastic about parallel computing (MPP). They would much rather have good big shared-memory machines. The PIs have made that point to NSF also.
our numbers say that there is no advantage to MPP, and it also takes a lot of work to use this technology.

10. Plans for an IBM SP2, spring 1994

NCAR almost obtained an IBM SP2 with 32 nodes that would have been delivered in July 1994. Each node would have 256 MB of memory (32 Mwords) and a 2-GB disk. The cost for 3 years, including maintenance, would be $2.4M ($800K per year). The power (if used in single-processor mode) would have been equivalent to about 10.9 Y-MP processors (32 nodes times 0.34 each). The output is probably only 20% of this much if used in parallel mode, unless I/O and calculations can be overlapped. On initial timing tests in early 1994, a node on the SP2 was much faster than a node on the Cray T3D. Other interesting computing options came into focus at NCAR (especially the Cray EL shared memory computers). The plans and contracts for an SP2 (almost final) were dropped on May 12, 1994.

11. The DEC Alpha 21164 Chip (Oct 1994)

A new alpha chip will be in production soon (announced Sep 7, 1994). At 300 MHz it will give 330 SPECint 1992 and 500 SPECfp 1992. This is fast. It has 66% more floating point performance than the flashy MIPS R 8000/8010 chips available in products about Aug 1994. The 266 MHz version will sell for $1865 each in volume and be available in Jan 1995. The 300 MHz version will be available in volume in Mar 1995, and sell for $2669 each (for large quantities).

- The 300-MHz chip should be about 0.48 of a Y-MP processor on big models, and perhaps 0.55 of a Y-MP for average work.

The 21164 chip has 9.3 million transistors; many of these are for cache memory. The chip has four execution units and can issue up to two integer and two floating point instructions each cycle. It has a faster clock and more instruction units than the previous 21064 and 21064A. On some key operations it also requires fewer cycles per operation. The chip is built with a 0.5-micron process, but will probably move to a 0.35-micron process sometime in 1995. The chip is further described by Ryan (1994) in the Oct 1994 issue of BYTE magazine.

Alpha is a true 64-bit architecture. For comparison, Hewlett Packard machines achieve 64 bits by doubling up clock cycles in a 32-bit design.


12. The Cray 3

The Cray 3 is still at NCAR (Aug 1994). It has been down since June 1, 1994 (there was not enough cooling water for both this computer and the new Y-MP).

- We were only able to use 1 processor on the Cray 3 before (about 55% of the time).
- In Sep 1994, Cray will put 2 of the new processors in the Cray 3 at NCAR and we will use them. This new, improved Cray 3 was powered up on 23 Sep 1994.

- 6 -
• The development of the Cray 4 is coming along, perhaps something will be going by late fall 1994.

13. The Power PC 620

The Power PC 601 was introduced in fall 1993. In early 1994 the 604 came on stage, a high-performance 32-bit processor. The 620 is the first 64-bit implementation of the Power PC architecture. It is targeted for workstations and high-speed servers. At 133 MHz the 620 achieves 225 SPECInt 92, and 300 SPECfp 92. It uses 0.5-micron technology, operates at 3.3μ like the 603 and 604, and uses 7 million transistors, nearly double the 604 design. Apple uses the 601 in Power Macs, and sold over 345,000 units in only 4 months. IBM shipped its one millionth 601 chip in July 1994, after just 10 months of production. The 620 will appear in computers in the second half of 1995. For more information, see the 5-page article in the Nov 1994 issue of Byte magazine, by Tom Thompson and Bob Ryan.

14. The Cray 4; A New Low-cost Tiger from Seymour Cray?

Seymour Cray said that a new Cray 4 with 8 processors will have the power of existing supercomputers that cost $24 million, but it will cost $4 million. The 8-processor Cray would probably have the same power as 33 Y-MP processors. (This is the same power as a Cray C-90 with 16 processors.) Let us hope that this Cray 4 development succeeds! An interview of Cray was in the July 18, 1994, Computerworld. A few of the questions and answers (shortened somewhat) follow:

Q: What is holding back the widespread use of so-called massively parallel supercomputers?

A: Seymour Cray: There are two issues. One is software—It's hard to program a lot of processors. And the other is hardware—how do you get good communications? When you have a lot of processors interconnected without a common memory, it's very difficult to get high transfer rates.

Q: What else is coming in high-performance computing?

A: We will have a Gflops in a desktop computer very soon. Then supercomputer centers will have a more specialized role than just running 500 users a day in time-sharing mode. They will run a few huge jobs, but the rest will be better off on the desktop. (But Cray does not plan to make these desktops.)

Q: What is the future of silicon processors?

A: I think somewhere around 500 MHz they are going to run into really basic problems. Then they will have to use gallium arsenide or something else.

Q: Why has Cray Computer gotten off to such a slow start?
A: We couldn't get any of the machine tools we needed, so we had to develop them. I tried three times to work with gallium arsenide facilities elsewhere but was not successful. So we now have our own gallium arsenide foundry here.

Q: Are you ready to release commercial products?

A: The Cray 3 was the vehicle for getting all these things hooked together, a prototype for the Cray 4. As a result, we came too late to market; it wasn't dramatic enough (in performance) at the point in time we could deliver it. But there does seem to be an opportunity now to move on to the Cray 4 because we have the infrastructure in place.

Q: What will the Cray 4 be like?

It will perform the same functions as existing $24 million (supercomputers) for $4 million. It is a conventional multiprocessor vector machine with a common memory, a close cousin to the Cray 3 and the C-90 and Y-MP (from competitor Cray Research). It will have a 1 nsec clock period (1000 MHz). The $4 million machine would have eight processors and 4 Gbytes of very fast (20 nsec static random-access) memory.

Q: When will it be available?

A: Early next year (1995); we want to demonstrate a system by year's end (Dec 1994).

Q: What can you say about the Cray 5?

A: It will have 2,000-MHz processors.

Q: Cray Research has said its new vector supercomputer will be out in late 1995 or early 1996. How will its performance compare to the Cray 4?

A: I think it is only half as fast (as the Cray 4). I'm looking forward to that competition because I think a factor of two is enough that we can compete.

Q: What is Cray Computer's financial status?

A: We just finished an asset-based financing. We have about $40 million in assets (and) we are spending $2 million to $3 million a month. We need to get a product recognized in the marketplace to get equity financing early next year in order to keep going.

Q: Can you afford to send $300 million-plus on each development cycle as you have for the Cray 3?

A: Oh, no. That's a onetime event. We can take our existing production capability another step beyond the Cray 4 with large-scale integration. I'm looking for a factor of four performance improvement in each (four-year development cycle), and I think we can do it within the $3 million-per-month budget.
Q: What accomplishment are you most proud of?

A: The first thing I did that I think was kind of outstanding was the Control Data 6600. At that point in time (1963), IBM imagined itself as going to completely dominate the (scientific computing) market. But the 6600 was quite successful, and I know that caused frustration among the IBM folks. There's satisfaction at having a little company be successful where a big one seems not able to.

Q: You once said you had given up using specific design tools in favor of intuition. How important is intuition in your work today?

A: It's intuition plus feedback from users.

Q: Do you plan to retire soon?

A: That frightens me. I will work as long as I am able. I need a successor, and I have several candidates, young people here.

15. A Longer Exabyte Tape (7 Gbytes)

About July 1994 Exabyte started selling a longer tape: 160m compared to 112m before. This tape will hold about 40% more data, giving 7 Gbytes instead of 5 now (not using compression). The tape drive is the same, but apparently it will be called the 8505 XL. This information is from Mike Duffer, Exabyte Marketing, 303-447-7179.

16. Sun Computers with Multiple Processors (July 1994)

The NOAA climate center in ERL-Boulder recently obtained two Sun Sparc computers, each with 8 CPUs. One computer has 1 GB of memory and the other one has 0.5 GB of memory. Each box of 8 CPUs has access to 75 GB of disks (150 total). Each CPU runs at 50 MHz and runs Linpack at a rate of about 30 Mflops. The SPECfp 1992 rating is probably about 100. These computers and disks cost about $400,000 on an upgrade; the outright purchase cost would have been about $500,000. The new processor will be ready by December 1994; it will be twice the speed (run at 100 MHz). They are also obtaining 30 GB of RAID disks that will cost $34,000 (GSA cost).

This NOAA climate group is also obtaining a mass store that uses optical disks from Hewlett Packard. It will have 144 platters and 4 drives. The disks are erasable optical, and read and write data at 1 MB/sec. A new platter can be mounted in 11 sec. The 144 platters hold a total of 187 GB now (July 1994), but will hold twice as much in a year. The GSA cost is only $34,000, but it does not include the platters. The GSA cost of 8 platters is $599.
The Speed of Recent Computer Chips

The capability of recent "small" computer chips is amazingly good. Table 1 summarizes information about these chips and the timing tests, SPECint and SPECfp. These timing tests each include about 10 to 20 different code modules, and seem to give a fairly good relative idea about how well big model codes will run on the computers.

On 24 May 1994, IBM announced the 380 and 390 machines. The 390 is the speed of a 6000/580H, yet a box with 32 MB of memory and 2 GB of disk costs only $18,830 for NCAR (the NCAR price is about 3% better than GSA government prices). The NCAR price for an IBM 590 is now $39,100, with 64 MB of memory and 2 GB of disk space. On May 24 IBM announced their 7015/R24 chip. It is the same as the 590 chip, but it has a little more cache so it is somewhat faster. The 590 runs a NCAR climate model at 0.29 the speed of one processor of a Cray Y-MP.

In late 1994, IBM will announce their new shared memory computer with 1 to 8 processors. Sometime in 1995 it will be available with the new 620 chip, which is the follow-on to the Power 2 line. With this chip they will have a full 64-bit capability. The present IBM chips are fast in doing 64-bit floating point calculations, but the 620 chip will be fully 64 bit (14 Jul 1994, Randy Hamann, IBM, 773-5421).

The SPEC Computer CPU Timing Tests

The SPEC timing tests use a typical mix of programs and average the results to produce a measure of performance. The MIPS benchmark was popular for awhile, but is not too accurate and has trouble when applied to RISC chips. Manufacturers tried to get around this by defining an equivalent VAX MIPS, but even this had trouble. A group of companies—including IBM, DEC, HP, Intel and Sun—established the System Performance Evaluation Corp. (SPEC). An original SPEC 89 suite of timing programs was first released. The SPEC 92, Release 1.1 has 20 programs used in the benchmarks. Six of these are used for integer speeds and the other 14 are for floating point. The reference value for SPEC is the execution time of a VAX-11/780, a very popular model for many technical people in the mid-1980s. The VAX-11/780 could compute at a rate of about 1 MIPS (integer) and 0.25 Mflops (floating point). For more information, see Sharp and Bacon, 1994.

Table 1. Speed of Selected Computer Chips

<table>
<thead>
<tr>
<th>Date of Technology</th>
<th>Chip</th>
<th>MHz</th>
<th>SPECint 92</th>
<th>SPECfp 92</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM power line</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jun 1991</td>
<td>6000/550</td>
<td>42</td>
<td>36.2</td>
<td>81.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6000/580</td>
<td></td>
<td>61.7</td>
<td>133.2</td>
<td></td>
</tr>
<tr>
<td>Oct 1993</td>
<td>6000/580H</td>
<td>50</td>
<td>97.6</td>
<td>203.9</td>
<td>Uses new compiler (18% gain)</td>
</tr>
<tr>
<td>Nov 1993</td>
<td>6000/590</td>
<td>66</td>
<td>117</td>
<td>242</td>
<td>First Power 2</td>
</tr>
<tr>
<td>~Feb 1994</td>
<td>6000/990</td>
<td>72</td>
<td>126</td>
<td>260</td>
<td></td>
</tr>
<tr>
<td>May 1994</td>
<td>7015/R24</td>
<td>66</td>
<td>130.3</td>
<td>270.8</td>
<td></td>
</tr>
<tr>
<td>Aug 1993</td>
<td>SP1</td>
<td></td>
<td></td>
<td></td>
<td>83% of the 580 speed</td>
</tr>
<tr>
<td>Aug 1994</td>
<td>SP2</td>
<td>66</td>
<td>117</td>
<td>242</td>
<td>Same as 590</td>
</tr>
<tr>
<td>May 1994</td>
<td>390</td>
<td>67</td>
<td>113.2</td>
<td>204.3</td>
<td>NCAR cost $18.8K</td>
</tr>
<tr>
<td>MIPS chips, Silicon Graphics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jun 1993</td>
<td>R4400SC</td>
<td>100</td>
<td>58</td>
<td>62</td>
<td>65% of the IBM 580</td>
</tr>
<tr>
<td>Dec 1993</td>
<td>R4400SC</td>
<td>150</td>
<td>86</td>
<td>93</td>
<td>90% of the IBM 580</td>
</tr>
<tr>
<td>before May 1994</td>
<td>R4600PC</td>
<td>133</td>
<td>92</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td>e Jul 1994</td>
<td>R4400*</td>
<td>200</td>
<td>108</td>
<td>310</td>
<td></td>
</tr>
<tr>
<td>e Aug 1994</td>
<td>R8000</td>
<td>75</td>
<td>108</td>
<td>310</td>
<td></td>
</tr>
<tr>
<td>DEC Alpha</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21066</td>
<td>166</td>
<td>70</td>
<td>105</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21064</td>
<td>200</td>
<td>130</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e Aug 1994</td>
<td>21064A</td>
<td>275</td>
<td>e 175</td>
<td>e 270</td>
<td>A tiger</td>
</tr>
<tr>
<td>e Apr 1995</td>
<td>21164</td>
<td>300</td>
<td>330</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>Sun</td>
<td>Microspac II</td>
<td>100</td>
<td>63</td>
<td>56</td>
<td></td>
</tr>
<tr>
<td>Intel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oct 1992</td>
<td>486 DX2</td>
<td>66/33</td>
<td>32</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Aug 1993</td>
<td>586/Pentium</td>
<td>66</td>
<td>65</td>
<td>57</td>
<td></td>
</tr>
<tr>
<td>May 1994</td>
<td>Pentium</td>
<td>100</td>
<td>100</td>
<td>80.6</td>
<td></td>
</tr>
<tr>
<td>(P54C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power PC (IBM, Motorola)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nov 1993</td>
<td>PowerPC 601</td>
<td>80</td>
<td>85</td>
<td>105</td>
<td></td>
</tr>
<tr>
<td>e Nov 1994</td>
<td>PowerPC 604</td>
<td>66</td>
<td>160</td>
<td>165</td>
<td></td>
</tr>
<tr>
<td>??</td>
<td>PowerPC 620</td>
<td>133</td>
<td>225</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>

* Estimated about 20% faster than an IBM 580. On standard Microsoft windows applications, this chip was 3.08 times faster than an Intel 90 MHz Pentium chip. But I doubt that floating point is as good as a 580 chip.

The date is the approximate date when the chip first appeared in products. The Intel and Power PC chips are being used in large numbers of PCs. These computers are low in cost, but they are still fast. The MIPS R8000 chip is used in Silicon Graphics shared memory computers. Wholesale prices of chips in lots of about 1000 are:


IBM representative: Randy Hamann, 773-5421
# MIPS CPU UPDATE*

<table>
<thead>
<tr>
<th></th>
<th>R3000</th>
<th>R4000PC</th>
<th>R4600PC</th>
<th>R4000sc</th>
<th>R4400sc</th>
<th>R8000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock(Mhz)</td>
<td>33</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>150</td>
<td>75</td>
</tr>
<tr>
<td>P Cache(i/d,kb)</td>
<td>64/64</td>
<td>8/8</td>
<td>16/16</td>
<td>8/8</td>
<td>16/16</td>
<td>16/16</td>
</tr>
<tr>
<td>Sec. Cache</td>
<td>none</td>
<td>none</td>
<td>none</td>
<td>1MB</td>
<td>1MB</td>
<td></td>
</tr>
<tr>
<td>MIPS</td>
<td>30</td>
<td>87</td>
<td>119</td>
<td>88</td>
<td>135</td>
<td></td>
</tr>
<tr>
<td>MFlops</td>
<td>4.2</td>
<td>5.9</td>
<td>11</td>
<td>16</td>
<td>24</td>
<td>101</td>
</tr>
<tr>
<td>SPECint92</td>
<td>22</td>
<td>36</td>
<td>63</td>
<td>58</td>
<td>86</td>
<td>108</td>
</tr>
<tr>
<td>SPECfp92</td>
<td>24</td>
<td>37</td>
<td>50</td>
<td>62</td>
<td>93</td>
<td>310</td>
</tr>
<tr>
<td>Date in products</td>
<td>Aug'93</td>
<td>mar'94</td>
<td>Aug'93</td>
<td>Dec'93</td>
<td>Aug'94</td>
<td></td>
</tr>
</tbody>
</table>

Note: ** indicates kilobytes for instructions / data

*For a given cpu, specs may differ slightly between systems

(This information was from John Brandan, Silicon Graphics, Denver office July 1994)

SGI 796-0022 Denver
<table>
<thead>
<tr>
<th>MODEL</th>
<th>IBM 25T</th>
<th>HP 715/550</th>
<th>SUN LX</th>
<th>DEC* 300L</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRICE ($)</td>
<td>9,395</td>
<td>13,990</td>
<td>8,995</td>
<td>7,645</td>
</tr>
<tr>
<td>$/SPECint92</td>
<td>150</td>
<td>377</td>
<td>341</td>
<td>167</td>
</tr>
</tbody>
</table>

IBM 250EM disk. 16" color display. Operating system. "HP has a 16" display Performance as of 12/17/93

<table>
<thead>
<tr>
<th>DIGITAL</th>
<th>HP 9000</th>
<th>SUN</th>
<th>IBM</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROCESSORS</td>
<td>1-4</td>
<td>1-2</td>
<td>1-8</td>
</tr>
<tr>
<td>SPECint92</td>
<td>124.0 per CPU</td>
<td>108.8 per CPU</td>
<td>60.3</td>
</tr>
<tr>
<td>I/O (MB/sec.)</td>
<td>132</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>INTERNAL RAID</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>ENTRY PRICE (US $)</td>
<td>$26,900</td>
<td>$76,000</td>
<td>$46,700</td>
</tr>
</tbody>
</table>

What HP is offering with its new Unix workstations

<table>
<thead>
<tr>
<th>WORKSTATION</th>
<th>SPECint92/SPEC92</th>
<th>AVAILABLE</th>
<th>PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP 715 64 MHz</td>
<td>67/97</td>
<td>Now</td>
<td>$9,995</td>
</tr>
<tr>
<td>HP 715 80 MHz</td>
<td>84/121</td>
<td>Now</td>
<td>$13,600</td>
</tr>
<tr>
<td>HP 715 100 MHz</td>
<td>100/137</td>
<td>Now</td>
<td>$19,005</td>
</tr>
<tr>
<td>HP 725 100 MHz</td>
<td>100/137</td>
<td>Third quarter</td>
<td>Not available</td>
</tr>
</tbody>
</table>

Computerworld May 23, 1994 63
High-Performance Microprocessors: An Overview

<table>
<thead>
<tr>
<th>Design</th>
<th>Microsoft Windows NT currently available</th>
<th>Maximum clock speed</th>
<th>Price per chip</th>
<th>Register size</th>
<th>Operating voltage</th>
<th>Typical power consumption at maximum clock speed</th>
<th>Maximum number of instructions per cycle</th>
<th>Cache size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alpha 21064</td>
<td>Digital Equipment Corp.</td>
<td>200 MHz</td>
<td>$1,304</td>
<td>64-bit</td>
<td>3.3V</td>
<td>27W</td>
<td>2</td>
<td>16K (8K for code, 8K for data)</td>
</tr>
<tr>
<td>MIPS R4000</td>
<td>MIPS Technologies Inc.</td>
<td>150 MHz</td>
<td>$450-$600</td>
<td>64-bit</td>
<td>3.3V, 5V</td>
<td>10W (3.3V), 20W (5V)</td>
<td>1</td>
<td>32K (16K for code, 16K for data)</td>
</tr>
<tr>
<td>PA-RISC 7100</td>
<td>Hewlett-Packard Co.</td>
<td>99 MHz</td>
<td>Info not available</td>
<td>32-bit</td>
<td>5V</td>
<td>23W</td>
<td>2</td>
<td>N/A</td>
</tr>
<tr>
<td>Pentium</td>
<td>Intel Corp.</td>
<td>66 MHz</td>
<td>$898</td>
<td>32-bit</td>
<td>5V</td>
<td>13W</td>
<td>2</td>
<td>16K (8K for code, 8K for data)</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>Apple Computer Inc., IBM Corp., Motorola Inc.</td>
<td>80 MHz</td>
<td>$545</td>
<td>32-bit</td>
<td>3.3V</td>
<td>9W</td>
<td>3</td>
<td>32K (unified)</td>
</tr>
<tr>
<td>Sun SuperSPARC+</td>
<td>Sun Microsystems Inc.</td>
<td>50 MHz</td>
<td>$860</td>
<td>32-bit</td>
<td>5V</td>
<td>9.5W</td>
<td>4</td>
<td>36K (20K for code, 16K for data)</td>
</tr>
</tbody>
</table>

*In lots of 1,000. **In lots of 10,000. N/A—Not applicable. The product has no on-board cache.
Comparison of Cray EL and IBM 590  
(All results for 1 processor, and Mflop results for 64 bits unless stated otherwise)

<table>
<thead>
<tr>
<th>Test (MHz)</th>
<th>IBM 550 (42)</th>
<th>590 (66)</th>
<th>Cray Y-MP (33)</th>
<th>Cray Y-MP (166)</th>
<th>Ratio of the 590 to Y-MP</th>
<th>Ratio for the faster 590 Compiler (18%)</th>
<th>Ratio for EL to Y-MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shallow-256 (Mflops)</td>
<td>26</td>
<td>57</td>
<td>48</td>
<td>215</td>
<td>0.27</td>
<td>0.31</td>
<td>0.22</td>
</tr>
<tr>
<td>Shallow-64 (Mflops)</td>
<td>25</td>
<td>50</td>
<td>37</td>
<td>210</td>
<td>0.24</td>
<td>0.28</td>
<td>0.18</td>
</tr>
<tr>
<td>Browning/Kreiss (Mflops)</td>
<td>29</td>
<td>85</td>
<td>51</td>
<td>217</td>
<td>0.39</td>
<td>0.24</td>
<td>0.24</td>
</tr>
<tr>
<td>Linpack - 1000x 1000 (Mflops)</td>
<td>70</td>
<td>129</td>
<td>32</td>
<td>161</td>
<td>0.80</td>
<td>0.20</td>
<td>0.20</td>
</tr>
<tr>
<td>Memory test (MB/s)</td>
<td>71</td>
<td>166</td>
<td>774</td>
<td>2594</td>
<td></td>
<td>0.30</td>
<td>0.30</td>
</tr>
<tr>
<td>I/O test (MB/s, w/o COS blking)</td>
<td>4.0</td>
<td>2.4</td>
<td>1.0</td>
<td>13.8</td>
<td>0.29</td>
<td></td>
<td>0.29</td>
</tr>
<tr>
<td>I/O test (MB/s, w/COS blking)</td>
<td>4.0</td>
<td>2.4</td>
<td>1.0</td>
<td>13.8</td>
<td>0.29</td>
<td></td>
<td>0.29</td>
</tr>
<tr>
<td>ccm0b1 (cpu sec, 5-day run)</td>
<td>1691</td>
<td>–</td>
<td>888</td>
<td>187</td>
<td>e 0.26</td>
<td></td>
<td>0.21</td>
</tr>
<tr>
<td>(64-bit precision)</td>
<td>1626</td>
<td>716</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>(32-bit precision)</td>
<td>1691</td>
<td>–</td>
<td>888</td>
<td>187</td>
<td>e 0.26</td>
<td></td>
<td>0.21</td>
</tr>
<tr>
<td>stswm2 (cpu sec, 240 iter)</td>
<td>59.6</td>
<td>32.0</td>
<td>–</td>
<td>16.1</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(64-bit precision)</td>
<td>54.3</td>
<td>35.0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>(32-bit precision)</td>
<td>54.3</td>
<td>35.0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

Notes:

1 The IBM 590 results were run on the ACD 590 (with 7/93 compiler); the 64-bit case for ccm0b was not run because of insufficient disk space for scratch files used by the model.

2 For the stswm (spectral transform shallow water model Case 4), the IBM 590 is about 50% of a Y-MP processor. The stswm runs at 96 Mflops on the Y-MP, two inefficient routines performing nonvectorized complex arithmetic. This is slower than many codes on the Y-MP; therefore, the ratio of 0.50 (the 590 speed to the Y-MP) is probably higher than typical codes.

- For the 550 and 590, there is very little difference in performance between 32-bit and 64-bit precision for the shallow-256 and shallow-64 models.

- For the ccm0b code, the 590 is 2.3 times faster than the 550 for 32-bit precision. For the stswm, the 590 is 1.8 times faster than the 550.

- Results are from P. Rotar and R. Sato.
Cray rolls with supercomputing changes
Plant revamp will aid fast turnaround
By Craig Stedman

The changes afflicting the high-performance computing market as government demand declines and technology choices proliferate are forcing even supercomputer top dog Cray Research, Inc., to learn some new tricks.

Citing a need to expand sales of smaller systems to make up for flat revenue from its biggest supercomputers, Cray recently said it plans to temporarily shut down most of its Chippewa Falls, Wis., manufacturing plant in order to retool the facility for faster turnaround times on systems.

The staggered work stoppage will begin Oct. 10 and last four to eight weeks, although it is not expected to delay any scheduled 1994 deliveries to customers, Cray said. Once a new, more automated manufacturing process is in place, 382 of the 1,530 workers at the Chippewa Falls plant will be laid off, the company added.

Changing needs
The need to produce supercomputers more quickly — and to cut the cost of making them — is driven by the rise of massively parallel processors and increased competition from Unix systems and clustered workstations. “Our customers have choices today [that] they didn’t have just a few years ago,” wrote John Carlson, Cray chairman and chief executive officer, in a memo to employees about the upcoming manufacturing changes.

Cray said the retooling of the Chippewa Falls plant should reduce the manufacturing cycle on its high-end C90 systems from almost a year to 16 weeks. Turnaround times on the company’s smaller machines, including the soon-to-be-announced J90, will go from two months to “a month or less,” the vendor said.

Despite the layoffs, analysts said Cray Research is not in the same leaky boat as other high-performance computer vendors, such as spin-off Cray Computer Corp. and Thinking Machines Corp., which have been taking on serious water. Indeed, despite flat high-end sales, first-half profits for Cray Research increased a healthy 42% over 1993, while revenue rose 19%.

However, orders fell significantly in the first half (see chart). There were extenuating circumstances because of the timing of some large orders received in late 1993 and in July, and the drop-off has not hurt revenue yet because of the long lead times on supercomputers. But analysts noted that Cray is losing the luxury of being able to take orders up to a year before delivering systems — meaning it has to build them faster to avoid revenue hits.

“Cray had been in an incredibly comfortable position, but the world doesn’t work that way anymore,” said Jeffry Canin, a securities analyst at Salomon Brothers, Inc. in San Francisco. Even supercomputers have “become much more of a book-and-ship type of business,” he added.

Cautious optimism
Terry Bennett, director of technical systems research at Computer Intelligence/InfoCorp in La Jolla, Calif., said Cray has been slow to update its manufacturing operations. “They still handcraft a lot of their work, and they shouldn’t,” he said. The retooling “is a very sensible step to take.”

Cray has indicated that its ability to meet 1994 financial goals “is not without risk” because of the first-half order slippage. Canin agreed that while Cray appears to be weathering the high-performance storms in relatively good shape, “you have to keep a little guarded” on its short-term outlook.

Our customers have choices today that they didn’t have just a few years ago.
Raw power is lure in Cray's low-end bid

By Craig Stedman

Cray Research, Inc. is trying for the second time to establish itself as a force to be reckoned with for general-purpose industrial computing. This time around, Cray is offering considerably more raw power than it was able to muster in its first low-end supercomputers.

While Cray dominates the market for large supercomputers costing upward of $30 million, its 3-year-old smaller systems line has not been regarded as particularly supercharged. But Cray recently introduced a J916 low-end model that analysts said lives up to its name better than the earlier EL90.

Promised performance
"Based at least on the specifications, this looks to be a far more compelling product than its predecessor," said Gary Smaby, president of Smaby Group, Inc. in Minneapolis. "The price/performance just wasn't there" on the EL90 to give the system enough appeal in the broad technical market, he added.

Altair Engineering, Inc., an automotive design and analysis company in Troy, Mich., is satisfied with the two EL90s it has installed. But Neil Price, director of marketing at Altair, said the J916's promised threefold performance improvement should allow the company to widen its computing horizon.

"We've got classes of problems that won't even fit" on the EL90, Price noted. "The need for this type of analysis is growing, and we're getting bigger and bigger problems thrown at us all the time." Altair expects to be one of the first customers to get a J916 when it ships early next year, he said.

With the J916, "we could attempt to do things that we don't currently try," agreed Jon Knight, vice president and chief investment officer at Atlantic Portfolio Analytics and Management, Inc. (APAM), an investment company in Orlando, Fla. There are limits to how many simulation jobs his company can "comfortably run and store" on the four-processor EL90 that APAM owns, Knight added.

The J916's 4G-byte memory capacity is enticing compared with the 1G-byte limit on the EL90, Knight said. But he said APAM has not benchmarked the J916 yet and will not make any firm upgrade plans "until we see what kind of performance we can get" from the new hardware.

The EL90 machines have not exactly been a bust. Cray executives said more than 180 of the low-end systems have been installed since their 1991 debut, with about 140 of those going to customers who had never bought one of the company's big water-cooled supercomputers.

Not quite there
But analysts said sales have not met Cray's original expectations due in part to the 1992 collapse of a deal under which Digital Equipment Corp. was supposed to handle most of the marketing for the low-end machines. That forced Cray to depend on its much smaller sales force to try to break into new accounts.

Daniel Hogberg, general manager for small systems at Eagan, Minn.-based Cray, acknowledged that the EL90 machines have been "quietly successful." Low-end systems still bring in less than 10% of Cray's revenue, according to Hogberg. However, he added that the company plans to be more visible.

"Just plain old marketing has been kind of a foreign concept at Cray," Hogberg said. "We've been a word-of-mouth technology vendor and that works at the high end. But we need to make ourselves more broadly known" in order to compete more successfully for general-purpose industrial business.

There are a lot of other technical computing choices in the J916's price range, which runs from $225,000 to about $2 million. IBM and Silicon Graphics, Inc. both sell RISC multiprocessors in that market, and workstation clusters can also be used to run the compute-intensive simulations and design applications that the J916 is meant to address.

Altair previously relied on a network of "every supercharged workstation you can think of," but moving to Cray's vector supercomputers was "a major step forward," Price said. Small tasks are still handled by workstations, "but the Cray is the buldozer that we use to load up the big analysis jobs," he said.

Being competitive
Smaby noted, though, that Cray cannot depend simply on number-crunching capabilities to carry the day in the low-end market. "Machoflops are less important in this category than they are with the big iron," he said. "It all gets down to how competitive they are on specific applications."

The J916 runs the same instruction set as Cray's high-end systems and has about 600 third-party applications available as a result. While that number is small compared with the number of packages that run on workstations and RISC systems, Smaby said, Cray's count is purely technical while the other platforms include commercial applications.
News

Cray envisions new frontier
Supercomputer would perform 1 quadrillion operations per second

By Gary H. Anthes
COLORADO SPRINGS

The aging but irrepressible Seymour R. Cray is building a supercomputer with 2 million processors, far more than any on the market today. And that is just the beginning.

Cray, the 68-year-old chairman and chief executive officer of Cray Computer Corp., said that within the next four years he plans to introduce a machine with 32 million processors, a machine able to perform a mind-boggling million billion — 1 quadrillion — operations per second.

Cray’s 2 million-processor machine will not be for the number-crunching scientific applications found on his traditional vector supercomputers. It will be designed for image processing, in which all the processors perform the same instructions simultaneously but on different pieces of an image — an approach called “single instruction, multiple data,” or SIMD.

Cost-saving venture
The new machine will achieve high performance at a low price by combining a simple bit processor with 2K bits of memory on a single chip, Cray said. It will cost $12 million to build — or $6 per processor — compared with the tens of thousands of dollars per processor required for the next generation of conventional vector computers.

Paul H. Smith, manager of NASA’s high-performance computing and communications program, said the space agency has many image-processing applications suited for a SIMD computer with a large number of processors. “Two million is a big number, and that will be hard to do from an engineering point of view,” he said. “But . . . this is probably a vision we should listen to.”

Meanwhile, it is full-speed ahead for the Cray 4, the company’s next generation of vector supercomputers. Cray said in a recent interview. He outlined a plan to move the financially challenged firm past the finish line on the Cray 4 (see story page 20), but he declined to discuss funding sources for the “massively parallel” image-processing machine.

Really big show
A petaFLOPS (1 million billion floating-point operations per second) computer would have to times the capability of all the networked computers in the U.S. today, according to “Enabling Technologies for PetaFLOPS Computing,” a report from Caltech.

Concurrent Supercomputing Facilities at the California Institute of Technology in Pasadena.

Twenty-year plan
Cray said the market potential for both lines of computers might be about equal, an assessment supported in a soon-to-be-released report from a panel of 60 high-performance computing experts in government, industry and academia. The report, entitled “Enabling Technologies for PetaFLOPS Computing,” summarizes the conclusions reached in a recent workshop sponsored by the National Science Foundation, NASA and the U.S. Departments of Defense and Energy.

The group, tasked with developing a vision for computers able to perform at 1 million billion floating-point operations per second (petaFLOPS), said the goal can be met “at reasonable cost with technology available in about 20 years . . . without the paradigms that exist today” (see chart).
Intel Cuts Pentium Chip Prices More Than 38%

SANTA CLARA, Calif. (Bloomberg) — Intel Corp., attempting to entice personal computer buyers toward Pentium-based systems, slashed third-quarter prices on its low-end Pentium chips by more than 38%.

The move comes as Intel aggressively tries to present Pentium as the standard chip for PCs, eating into the market of companies that make clones of Intel's previous-generation 486 chips.

Intel's 486 and Pentium chips are members of its x86 family of microprocessors, the brains inside an estimated 75% of the world's personal computers.

In a price list released Tuesday, Santa Clara-based Intel indicated that it will make a break with its usual practice and cut prices twice in the current quarter. For lots of 1,000 chips, Intel cut Pentium 60 MHz chip prices to $418 effective Aug. 1 from $675 in the second quarter. The 66 MHz Pentium was priced down to $525 from $750 in the second quarter.

Intel has said it will cut prices to allow PC makers to sell CD-ROM-capable Pentium-based systems starting at $2,000 by Christmas. Prices of such sophisticated systems now start at about $2,300.

Digital cuts Alpha prices, surfs the 'net

Digital Equipment Corp. is cutting prices on its Alpha AXP microprocessor this week, effective July 3. Prices range from $186 for the 21068 66-MHz chip to $1,088 for the 21064A 275-MHz model. Separately, the company said users can now order products and obtain software patches via the Internet. Digital has also signed a licensing agreement with Spyglass, Inc. to bundle Mosaic, an Internet navigation tool, on all of its Alpha AXP and Intel Corp.-based systems.

Chipping away at PC prices

Personal computer prices could plunge later this year, although computer makers don't expect an all-out price war.

Prices have been drifting lower all year. And Compaq, the PC maker that's become a price trendsetter, has lowered prices on several models.

Fueling the trend:

- Falling chip prices.
- Microprocessors, the brains of a PC, account for up to 35% of the cost of making a PC. And Intel, the dominant microprocessor maker, has been cutting chip prices aggressively.
- That has allowed PC makers to cut expenses and pass savings on to buyers.

The Santa Clara, Calif.-based company is battling unprecedented competition from companies such as IBM and Motorola as well as smaller firms like Advanced Micro Devices that clone Intel chips.

Intel wants to make its most powerful chip line, the Pentium, a hit as soon as possible. That means even more aggressive price cuts. Already, Pentium-based computers are available for around $2,500, about 20% to 25% cheaper than they were six months ago.

Intel officials say Pentium sales are being powered by people buying PCs for home use. They're drawn by the Pentium's raw computing speed.

- Excess supply. The past year, PC prices have been buoyed by supply shortages. Top companies such as Compaq and IBM have been struggling to crank out PCs to keep up with demand.

Now "some pockets of excess supply are starting to crop up," says Richard Zwetchkenbaum, analyst at International Data. So PC makers may ease prices to sell built-up stock of PCs and to pave the way for Pentium-based computers.

- Compaq has cut prices. The Houston-based PC maker increasingly sets the tone for other makers. And "it's making a strong statement," Zwetchkenbaum says.

Compaq's portable Contura Aero, priced at $1,395 when it was launched in February, now costs $995, 29% less. Also, prices on two popular PCs in its Presario line also were cut, by 15% and 25%, to $1,299 and $1,599. Both have compact-disk drives to run programs rich in video and animation. In all, prices were pared 4% to 29%.

In June 1992, Compaq started an all-out price war when it slashed prices across the board. This time, other PC makers aren't matching its cuts, though they might have to later. "We don't think we're going to have to respond," says Brent Cohen, chief operating officer of PC maker Packard Bell. "But we'll keep a close eye on the market."

Computer consultant Seymour Merrin notes, "The consumer wins in all this stuff."

— James Kim
HP lays out next-generation chip plans

Current offering receives power boost

By Mark Halper

Before Hewlett-Packard Co. moves to its "post-RISC" architecture, it has a few enhancements in store for its current PA-RISC, including a 125-MHz chip announced last week and a 64-bit, 200-MHz design due in mid-1995, the company said.

HP also provided details for the first time of its previously undisclosed plans for adding Windows NT support to PA-RISC and eventually moving to a new architecture [CW, Dec. 6, 13].

Users such as Dave Brolsma, manager of information systems at Chrysler Corp. subsidiary Acustar Electrical in El Paso, Texas, noted that while it is always encouraging to hear about faster chips, his near-term upgrade plans are for the desktop, not the enterprise server.

"The thing to remember is that as you move to client/server, you're pushing processing and the desktop, so you have to save somewhere," Brolsma noted. "I'm not sure I'll need more powerful servers in the background."

Ron Gillet, vice president of IS at Houston-based energy company The Coastal Corp., noted that he does not have an urgent need for more processor power, his interest in future processors will be based on pricing. "The bottom line is none of that directly impacts me unless it lowers my costs," Gillet said.

Jan Silverman, HP marketing manager for advanced technologies, last week said HP's move to a post-RISC processor, which will rely in part on Very Long Instruction Word (VLIW) technology, will come in 1997 or 1998. That move, which augurs chip performance of billions of instructions per second compared with today's millions, has raised concern among users over compatibility with existing PA-RISC software.

Silverman last week reiterated earlier HP statements that the company will ensure the new architecture is compatible with the old. But one of the most immediate PA-RISC changes is scheduled for next month when, Silverman said, HP will add a bi-endian version of PA-RISC and announce workstations (see story page 15) and minicomputers that use that chip, which will be called the PA-7100LC. HP said it also plans "a new class of LAN servers" built on the 7100LC.

Better little than big

The bi-endian chip is intended to move HP workstations and minicomputers into the Windows NT world via its "little endian" byte-ordering scheme, which arranges bytes in ascending order — a manner more suited for NT than HP's de-scending big endian-only design.

But the 7100LC was designed as a "low-cost" chip, and at a maximum of 80 MHz, does not offer the performance levels of faster PA-RISC processors. HP has earmarked it for low-end workstations and minicomputers.

Silverman pointed out, however, that the chip includes built-in multimedia support for image processing, a memory controller and an I/O controller, thereby reducing the cost of building that support on a system motherboard. The chip also uses off-the-shelf static RAM for cache support, compared with the more expensive RAM the 7100 requires.

Meanwhile, HP is cranking up the speed of the 99-MHz 7100 to 125 MHz in a chip intended solely for workstations. Called the PA-7150, the chip will continue in the 7100's big endian-only vein, meaning it is not intended to support NT.

But HP has another processor on the drawing board, the PA-7200, that will provide NT support through a bi-endian design while also representing a performance boost, Silverman said.

The PA-7200 is due in late 1994 or early 1995 and will include higher bandwidth, lower latency, a dual-integer pipeline and more efficient cache management, he said. HP will move to a 64-bit design in 1995 with the PA-8000 and to post-RISC in 1997 or 1998 with the PA-9000, Silverman said.
IN 1965, INTEL CO-FOUNDER GORDON MOORE PREDICTED TRANSISTOR DENSITY ON MICROPROCESSORS WOULD DOUBLE EVERY TWO YEARS. THIS PREDICTION, SO FAR, HAS PROVEN AMAZINGLY ACCURATE. IF IT CONTINUES, INTEL PROCESSORS SHOULD CONTAIN BETWEEN 50-TO-100 MILLION TRANSISTORS BY THE TURN OF THE CENTURY AND EXECUTE 2 BILLION INSTRUCTIONS PER SECOND. TO MEET THAT CHALLENGE, INTEL IS ALREADY DEVELOPING NEW TECHNIQUES TO FABRICATE THESE COMPLEX PROCESSORS.

WHAT THE INTEL INSIDE® LOGO REALLY MEANS.

COMPATIBILITY AND RELIABILITY.

This year, Intel will produce over 30 million processors, more than one processor every second. To achieve such high levels of production and still ensure quality, painstaking steps are taken to guarantee every processor is identical, and also compatible with over 50,000 software applications.

To begin, wafers are fabricated in “clean rooms.” These pristine environments prevent microscopic particles from damaging the wafers. Unlike a normal room, which contains some 15 million dust particles per cubic foot, an Intel clean room contains less than 1 dust particle per cubic foot. That’s why Intel workers wear “bunny suits” in the clean rooms.

Each new processor is also designed, manufactured and tested to be backwardly compatible with every other Intel processor, all the way back to our 8086 processor.

And finally, every Intel processor undergoes over one million functional tests to make sure it meets Intel’s standards for performance and reliability.

INVESTING IN TECHNOLOGY.

To ensure you’re always getting the most advanced processing technology, Intel invests heavily in the latest equipment and technology available. Each fabrication plant costs over $1 billion to construct, yet is considered obsolete after just five years. That’s how fast Intel is evolving its processor technology and one of the key reasons why Intel is the world’s #1 semiconductor manufacturer.
SIX YEARS OF PARALLEL COMPUTING
WHAT HAVE WE LEARNED?

Horst D. Simon
Computer Sciences Corporation
Applied Research Branch
NASA Ames Research Center

CRAY Executive Symposium, Scottsdale
April 1994

Mail Stop T27A-1
NASA Ames Research Center
Moffett Field, CA 94035-1000
simon@nas.nasa.gov
Overview

The last six years at NAS
Hardware/architecture
Applications
Algorithms
The state of HPC

1) 2) 3) 4) 5) 6)
### NAS Program Goals for Parallel Systems (1988)

<table>
<thead>
<tr>
<th>Year of Installation</th>
<th>System</th>
<th>Sustained Computing Rate (GFLOPS)</th>
<th>Peak(^1) Computing Rate (GFLOPS)</th>
<th>Main Memory (Gbytes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1989</td>
<td>Gen 1</td>
<td>1</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>1991</td>
<td>Gen 2</td>
<td>10</td>
<td>100</td>
<td>8</td>
</tr>
<tr>
<td>1994</td>
<td>Gen 3</td>
<td>200</td>
<td>2000</td>
<td>200</td>
</tr>
<tr>
<td>1997</td>
<td>Gen 4</td>
<td>2000</td>
<td>20000</td>
<td>1000</td>
</tr>
</tbody>
</table>

\(^1\) Maximum rate that is assumed necessary to reach stated sustained rate

\(^2\) Computing rates and memory capacities are for full-scale systems.
Growth in Processing Power at NAS

peak advertised performance in Gflop/s

[Diagram showing the growth in processing power at NAS over time, with different computers and years indicated]
Growth in Processing Power at NAS

speed measured in NPB BT equivalent Gflop/s

YMP/8 = 1.0
Cray 2 = 0.4
all others scaled according to NPB BT
NAS Growth in Workstations

Data hard to come by!

Total number of workstations at NAS

<table>
<thead>
<tr>
<th>Year</th>
<th>Count</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>1988</td>
<td>45</td>
<td>estimate based on UIG</td>
</tr>
<tr>
<td>1989</td>
<td>51</td>
<td>estimate based on UIG</td>
</tr>
<tr>
<td>1990</td>
<td>115</td>
<td>config. diagram count</td>
</tr>
<tr>
<td>1991</td>
<td>104</td>
<td>config. diagram count</td>
</tr>
<tr>
<td>1992</td>
<td>248</td>
<td>config. diagram count</td>
</tr>
<tr>
<td>1993</td>
<td>300</td>
<td>DCT statistic</td>
</tr>
</tbody>
</table>

On December 1, 1993 the aggregate workstation compute power was about 2.3 Gflop/s on the NAS workload benchmark.
Summary on Developments at NAS

NAS continues to rely on traditional parallel vector processors as main computational resource.

Unlike other installations NAS has not (yet) made a major investment in a highly parallel system.

The potential of distributed computing using high end workstations has only been realized very recently.
Overview

1) The last six years at NAS
2) Hardware/architecture
3) Software
4) Applications
5) Algorithms
6) The state of HPC
Lesson 1:

There are few "massively" parallel computers available, and there will be even less parallelism in the near future.
The trend away from "massively" parallel

The Teraflop barrier will be crossed in this region
$100 < p < 10,000$

Mflops per processor
The trend away from "massively" parallel

Reasons:

- powerful microprocessors are optimal design point

- the less parallelism the better

At NAS:

- we won’t have any machine with more than 1024 processors in the next five years

Trivia question: how many machines with more than 1023 processors, and more than 5Gflop/s peak are installed world-wide?
Lesson 2:

SIMD architectures (defined as tightly synchronized, massively parallel machines, built from not very powerful processors) have failed in general purpose scientific computing.
The end of SIMD – as we know it

Experience at NAS (1992):

Chawla using overset grid Navier–Stokes solver (CM3D by Jespersen and Levit) on 8K of CM–2:

Performance is extremely grid sensitive

magic size grid 64x64x64: 29 microsec/pt/step
generic size 70x56x70: 70 microsec/pt/step
recommended 70x64x72: 35 microsec/pt/step
User Acceptance of Parallel Machines

SIMD / CM-2

MIMD / iPSC860

performance

months

2 4 6

performance

months

2 4 6
The end of SIMD – as we know it

Reasons:
- SIMD implementations were not flexible enough
- High variability of performance
Lesson 3:

"Killer Micros" were the enabling technology for the rapid growth of highly parallel systems.
Growth in Microprocessor Performance in the 1980s

In the 1980s there have been fundamental changes in the microprocessor development ("killer micros")

- dramatic increase in number of transistors available per chip

- architectural advances including the use of RISC ideas, pipelining and caches

- as a result CPU performance has improved by a factor of 1.5 to 2.0 per year

Trivia question: how many instructions did the CDC 7600 have?
<table>
<thead>
<tr>
<th></th>
<th>Alpha</th>
<th>RS6000</th>
<th>i860</th>
<th>Y-MP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>150 MHz</td>
<td>62.5 MHz</td>
<td>40MHz</td>
<td>167MHz</td>
</tr>
<tr>
<td>divide clocks</td>
<td>63</td>
<td>20</td>
<td>38</td>
<td>4</td>
</tr>
<tr>
<td>cache size</td>
<td>8</td>
<td>64</td>
<td>8</td>
<td>none</td>
</tr>
<tr>
<td>memory bandwidth (Mwords/sec)</td>
<td>37.5</td>
<td>125</td>
<td>17</td>
<td>500</td>
</tr>
<tr>
<td>peak MFlops</td>
<td>150</td>
<td>125</td>
<td>60</td>
<td>330</td>
</tr>
<tr>
<td>ratio</td>
<td>0.25</td>
<td>1.0</td>
<td>0.28</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Scientific applications need at least a ratio of 1.0.

Alpha repeats the mistakes of the i860.
Current Acceptance of Custom and Commodity Processors

Custom/proprietary
- KSR
- Neube
- Masspar
- Fujitsu
- Tera

Semi-custom
- TMC
- Cray T3D
- Meiko

Commodity
- Intel
- Convex 411F
- IBM
- SGI
Future Use of Custom and Commodity Processors

In the near future there will continue to be a performance gap of about an order of magnitude between high performance custom processors and high performance commodity micro processors.

Therefore we will continue to see them both in high performance architectures.

The difference will be simply a degree of parallelism, i.e. 64 processors at 2Gflop/s versus 512 processors at 256 Mflop/s.
Lesson 4:

It's the interconnect – stupid.
## Bisection Bandwidth and Memory Bandwidth

<table>
<thead>
<tr>
<th>Machine</th>
<th>#proc</th>
<th>Bisection bw</th>
<th>Bisection bw/proc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cray T3D</td>
<td>128</td>
<td>9.6 GB/sec</td>
<td>75 MB/sec</td>
</tr>
<tr>
<td>IBM SP-1</td>
<td>64</td>
<td>3.2 GB/sec</td>
<td>50 MB/sec</td>
</tr>
<tr>
<td>Intel Paragon</td>
<td>208</td>
<td>3.2 GB/sec</td>
<td>16 MB/sec</td>
</tr>
<tr>
<td>CM-5</td>
<td>128</td>
<td>1.3 GB/sec</td>
<td>10 MB/sec</td>
</tr>
<tr>
<td>Cray C90</td>
<td>1</td>
<td>11.5 GB/sec memory bw</td>
<td></td>
</tr>
</tbody>
</table>

Note that these are "peak" numbers for the machines!
Bisection Bandwidth and Memory Bandwidth

Compute the "connectivity cost per node" for the parallel machines as follows:

Customer cost/processor = list price/\# processors, e.g. for 128 proc T3D
customer cost/processor = \$5.5M/128 = \$43K

Subtract memory cost (\$70 per 4Mbit DRAM) and processor cost (estimated between \$1000 and \$10K).

Result:   T3D     \$35K
           SP-1    \$25K
          Paragon \$20K
          CM-5    \$20K
Bisection Bandwidth and Memory Bandwidth (cont.)

Note "connectivity cost per node" correlates well to bisection bandwidth.

For comparison on the C90, 70% of the Cray designed hardware goes into the memory interface.

By a similar calculation the "memory interface cost" for a single processor of the C90 is of the order of $1M.

What do we learn? You don't get anything for free, especially not bandwidth.
## Networking Technology for Workstations

<table>
<thead>
<tr>
<th>Technology</th>
<th>Year</th>
<th>Bandwidth</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet</td>
<td>1981</td>
<td>10 Mbit/sec</td>
<td>$100</td>
</tr>
<tr>
<td>FDDI</td>
<td>1989</td>
<td>100 Mbit/sec</td>
<td>$1K – $2K</td>
</tr>
<tr>
<td>ATM DS−3</td>
<td>1993</td>
<td>45 Mbit/sec</td>
<td>$1,500</td>
</tr>
</tbody>
</table>

### in the near future

<table>
<thead>
<tr>
<th>Technology</th>
<th>Year</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATM OC−3</td>
<td>1994(?)</td>
<td>155.2 Mbit/sec</td>
</tr>
<tr>
<td>ATM TAXI</td>
<td>1994(?)</td>
<td>100/140 Mbit/sec</td>
</tr>
</tbody>
</table>

### in two years

<table>
<thead>
<tr>
<th>Technology</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATM OC−12</td>
<td>622.1 Mbit/sec</td>
</tr>
</tbody>
</table>

At the time of availability ATM cards plus cost of hub will cost about $5K – $10K per workstation.
## Networking Technology for Workstations

<table>
<thead>
<tr>
<th>MPP System</th>
<th>networked workstation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processors</td>
<td>comm. micro</td>
</tr>
<tr>
<td>Memory</td>
<td>comm. DRAM</td>
</tr>
<tr>
<td>Interconnect</td>
<td>vendor supplied</td>
</tr>
<tr>
<td>Cost of interc.</td>
<td>$20 - $30K</td>
</tr>
<tr>
<td>System softw.</td>
<td>vendor supplied</td>
</tr>
<tr>
<td>comm. micro</td>
<td>comm. DRAM</td>
</tr>
<tr>
<td>comm. ATM</td>
<td>$5 - 10K</td>
</tr>
<tr>
<td>your own or</td>
<td>research type</td>
</tr>
</tbody>
</table>

Since bandwidth, connectivity, and cost are about the same, the main discriminator is software. MPP systems provide a unified system image for the same type of hardware. If independent software developers or MPP vendors provide system software, then networked workstations will be winner.
Latency or Bandwidth?

Study by Van Voorst, Seidel, and Barsczc at NASA. Based on communication data for 14 days on iPSC/860 in production use.

<table>
<thead>
<tr>
<th>COMMUNICATION SPEEDUP</th>
<th>Bandwidth in Mbyte/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency in microsec</td>
<td>2.8 10 20 40 80 160</td>
</tr>
<tr>
<td>75</td>
<td>1.0 2.2 2.8 3.2 3.5 3.6</td>
</tr>
<tr>
<td>50</td>
<td>1.2 2.7 3.7 4.5 5.0 5.3</td>
</tr>
<tr>
<td>25</td>
<td>1.3 3.6 5.4 7.3 8.9 10</td>
</tr>
<tr>
<td>1</td>
<td>1.4 5.0 10 19 36 64</td>
</tr>
</tbody>
</table>

On current machines:

<table>
<thead>
<tr>
<th>Cray T3D (SHMEM_GET, PUT)</th>
<th>lat</th>
<th>bw</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM SP–2</td>
<td>40</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>30/120</td>
</tr>
</tbody>
</table>
Conclusions on Interconnects

High bandwidth interconnects remain the major challenge for MPP systems.

We continue to have the "Tflops" hangup, and focus attention on the wrong issue.

However, clustered workstations will provide an efficient throughput system for small and medium range jobs.

Latency is more critical than bandwidth for system performance.
Overview

1) The last six years at NAS
2) Hardware/architecture
3) Software
4) Applications
5) Algorithms
6) The state of HPC
Lesson 5:

Software remains the major problem area, we have not learned much.
Current Status: System Software

Montry – Worlton Iceberg Metaphor

Mature High Performance Systems

Massively Parallel Computing System
Evolution in Programming Models

1988
single architecture
single programming model

1993
single architecture
multiple programming models

199?
multiple architectures
multiple programming models
Lesson 6:

There are no new exciting massively parallel algorithms. Implementation of the best serial algorithms was sufficient (and difficult enough).
# Algorithms: MFLOPS vs. Run Time

## NCUBE-2 Performance on a Convection-Diffusion Problem (Shadid and Tuminaro, Sandia Natl. Lab.)

<table>
<thead>
<tr>
<th>Solver Algorithm</th>
<th>Floating Point Operations</th>
<th>CPU Time (Secs.)</th>
<th>MFLOPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jacobi</td>
<td>$3.82 \times 10^{12}$</td>
<td>2124</td>
<td>1800</td>
</tr>
<tr>
<td>Gauss-Seidel</td>
<td>$1.21 \times 10^{12}$</td>
<td>885</td>
<td>1365</td>
</tr>
<tr>
<td>Least Squares</td>
<td>$2.59 \times 10^{11}$</td>
<td>185</td>
<td>1400</td>
</tr>
<tr>
<td>Multigrid</td>
<td>$2.13 \times 10^{09}$</td>
<td>6.7</td>
<td>318</td>
</tr>
</tbody>
</table>

## Conclusions:

- When selecting an algorithm for a parallel computer, fundamental numerical efficiency is much more important than appropriateness for a particular architecture.

- Parallel computer systems must be designed to run numerically efficient algorithms at respectable performance rates.
Figure 4
Performance Improvement for Scientific Computing Problems

- Derived from Computational Methods
  - Multi-Grid
  - Conjugate Gradient
  - Successive Over-Relaxation
  - Sparse Gaussian Elimination

- Derived from Supercomputer Hardware
  - Vector Supercomputer

Speed-Up Factor
10^0
10^1
10^2
10^3
10^4

10^0
10^1
10^2
10^3
Vector Supercomputer

NONSENSE!
<table>
<thead>
<tr>
<th>Problem Size</th>
<th>INTEL iPSC/860</th>
<th>Cray-YMP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No. of Processors</td>
<td></td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>64</td>
</tr>
<tr>
<td>(24x24x24)</td>
<td>CE-GE</td>
<td>0.31</td>
</tr>
<tr>
<td></td>
<td>(87)</td>
<td>(159)</td>
</tr>
<tr>
<td></td>
<td>PGE</td>
<td>0.52</td>
</tr>
<tr>
<td></td>
<td>(52)</td>
<td>(81)</td>
</tr>
<tr>
<td></td>
<td>SGE-BCR</td>
<td>0.78</td>
</tr>
<tr>
<td></td>
<td>(37)</td>
<td>(42)</td>
</tr>
<tr>
<td>(40x40x40)</td>
<td>CE-GE</td>
<td>1.30</td>
</tr>
<tr>
<td></td>
<td>(104)</td>
<td>(202)</td>
</tr>
<tr>
<td></td>
<td>PGE</td>
<td>1.87</td>
</tr>
<tr>
<td></td>
<td>(72)</td>
<td>(123)</td>
</tr>
<tr>
<td></td>
<td>SGE-BCR</td>
<td>2.84</td>
</tr>
<tr>
<td></td>
<td>(48)</td>
<td>(68)</td>
</tr>
<tr>
<td>(80x80x80)</td>
<td>CE-GE</td>
<td>5.15</td>
</tr>
<tr>
<td></td>
<td>(219)</td>
<td>(428)</td>
</tr>
<tr>
<td></td>
<td>PGE</td>
<td>6.47</td>
</tr>
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<td></td>
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<td>(288)</td>
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<td>(150)</td>
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<td>(160x80x80)</td>
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<td>5.23</td>
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<td>(432)</td>
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<tr>
<td></td>
<td>(155)</td>
<td>(155)</td>
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</tbody>
</table>
Algorithms

Because of the absence of truly massively parallel machines, there has been no need to develop completely new algorithms.

The implementation of the best existing serial algorithms yielded in most cases the best results.

Implementation on parallel machines is far from trivial.

Algorithm work remains even more misunderstood than software.
Applications

Lesson 7:

We can classify applications according to their communications requirements. This classification is a good predictor of performance on parallel systems.
# Applications Performance as Measured by 'Gordon Bell Prize'

<table>
<thead>
<tr>
<th>Year</th>
<th>Gflop/s</th>
<th>flops/$</th>
<th>machine</th>
</tr>
</thead>
<tbody>
<tr>
<td>1987</td>
<td>0.45</td>
<td>30</td>
<td>nCUBE1</td>
</tr>
<tr>
<td>1988</td>
<td>1.0</td>
<td>50</td>
<td>Y-MP/8</td>
</tr>
<tr>
<td>1989</td>
<td>6.0</td>
<td>500</td>
<td>CM-2</td>
</tr>
<tr>
<td>1990</td>
<td>14.0</td>
<td>2000</td>
<td>CM-2</td>
</tr>
<tr>
<td>1992</td>
<td>7.1</td>
<td></td>
<td>192 wk</td>
</tr>
<tr>
<td>1993</td>
<td>60.0</td>
<td>7500</td>
<td>CM-5</td>
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</tbody>
</table>

Gflop/s here is the highest performance of any finalist, not necessarily the winning entry.

flops/$ here is the highest of any finalist, not necessarily the machine in column 2 and 4.
A Taxonomy for Parallel Applications

no or minimal communication

explicit (nearest neighbor) comm.

implicit (global) communication

embarrassingly parallel (EP)

explicit structured (ES)

explicit unstructured (EU)

implicit structured (IS)

implicit unstructured (IU)

structured communication

unstructured communication
A Taxonomy for Parallel Applications - dynamic

static explicitly structured (SES)
static implicitly structured (SIS)
static explicitly unstructured (SEU)
static implicitly unstructured (SIU)
embarrassingly parallel (EP)

DEU
DEU
DEU
DEU

DIS
DIS
DIS
DIS

DIU
DIU
DIU
DIU

dynamic during computation
static during computation
Difficulty of Parallel Implementation

easy

moderate

difficult

EP

SES

SIS

SEU

SIU

DES

DIS

DEU

DIU
Lesson 8:
High Performance Computing is of national importance.
National Importance of HPCC

1) HPC Technologies are indispensable for economic productivity and national security

2) Joint effort of HPCC agencies to accelerate the technology for civil and defense missions, education, science, and the environment

3) Collaboration with industry in broad national applications

4) On course towards 1000x increase in computing power and 100x increase in communications bandwidth

5) Presidential initiative – wide based support; part of wider vision of "change for America"
Current State of HPC Market

Number of Installations

30

Big Science

Installed Base

$500M

1,000

Production Engineering

$4,000M
The HPC Market (cont.)

<table>
<thead>
<tr>
<th>Number of Installations</th>
<th>Installed Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>$500M</td>
</tr>
<tr>
<td>Big Science</td>
<td></td>
</tr>
<tr>
<td>100% HPCC funding + 100% media attention</td>
<td></td>
</tr>
<tr>
<td>1,000</td>
<td>$4,000M</td>
</tr>
<tr>
<td>Production Engineering</td>
<td></td>
</tr>
</tbody>
</table>

The vendor's dilemma:
- competing in the big science market is not profitable
- competing in the big science market is important to build credibility
The HPC Market: failures and survivors

Out of business:
Alliant, American, Ametek, Culler, Cydrome, Denelcor, Elexsi, Multiflow, Myrias, Prisma, Saxpy, SCS, SSI(2), Trilogy, Wavetracer

Division closed:
Astronautics, BBN, CDC/ETA Systems, E&S, Gould, Vitesse

Merged:
Celerity, FPS, Key, Supertek

Down, not out:
AMT(Cambridge), CHoPP, Encore, Stardent/Kubota

Currently active:
Convex/HP, Cray Computer, Cray Research, Fujitsu, IBM, Intel, KSR, nCUBE, Meiko, NEC, Parsytec, SGI, Tera, TMC
## Current U.S. Leadership in HPC

### Top 50 supercomputers world wide

<table>
<thead>
<tr>
<th>Manufactured by</th>
<th>Installed in</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>U.S.</td>
<td>Japan</td>
<td>Europe</td>
<td>other</td>
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<tr>
<td>U.S.</td>
<td>39</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Japan</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

HPCC is needed to keep it that way. Remember the top 10 semiconductor manufacturer in 1980?
Views on Commercialization of MPP Technology

BACKGROUND

CBO report June 93: Discusses barriers to commercialization of HPCC technology. Leading up to a backlash against HPCC: NSF, ARPA HPCC budgets are cut.
The Facts About Industrial Use of MPP Technology

Industrial supercomputer installations based on the TOP 500 list, Nov. 1993

<table>
<thead>
<tr>
<th></th>
<th>Vector US</th>
<th>other</th>
<th>MPP US</th>
<th>other</th>
<th>Total</th>
</tr>
</thead>
<tbody>
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<td>0</td>
<td>0</td>
<td>29</td>
</tr>
<tr>
<td>Oil Industry</td>
<td>15</td>
<td>5</td>
<td>6</td>
<td>3</td>
<td>29</td>
</tr>
<tr>
<td>Aerospace</td>
<td>6</td>
<td>3</td>
<td>12</td>
<td>1</td>
<td>22</td>
</tr>
<tr>
<td>Electronics</td>
<td>2</td>
<td>10</td>
<td>3</td>
<td>4</td>
<td>19</td>
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<tr>
<td>Metal/Constr.</td>
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<td>10</td>
<td>0</td>
<td>0</td>
<td>10</td>
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<tr>
<td>Chem./Bio.</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>8</td>
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<tr>
<td>Econ./Finance</td>
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</tr>
<tr>
<td>Other</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>33</td>
<td>62</td>
<td>29</td>
<td>12</td>
<td>136</td>
</tr>
</tbody>
</table>
Views on Commercialization of MPP Technology

MPP’s have made major inroads in industry.

About 25% of all installed supercomputers are MPP’s.

The only genuine MPP success story is in seismic processing.

MPP’s have replaced PVP’s in traditional supercomputer markets, they have not (yet) opened new markets.
Price Performance on NPB

[Graph showing performance metrics with different labels and values]
Lessons learned: grossly simplified

1) There is no "massive" parallelism
2) SIMD did not work
3) Custom and commodity processors will both have their future
4) Bandwidth is the issue
5) Nothing has been learned in software
6) Good sequential algorithms do the job, but they are hard anyway
7) Not all applications are equal
8) This is important stuff!